



FPIC

FPGA Peripheral Interface Connector

Revision History

Revision	Date	Author	Description of Changes
V1.0	2026	Numato Systems	Initial release

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Compliance: Products displaying the FPIC designation **SHALL** fully conform to all mandatory (SHALL) requirements defined in this specification. Partial implementations SHALL NOT display the FPIC designation without clearly stating which variant (FPIC ST, FPIC GT4, FPIC GT8) is supported and which requirements are not met.

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1. Abstract

This standard defines the FPIC (FPGA Peripheral Interface Connector) module interface and establishes the mechanical, electrical, and signalling framework required for connecting compact peripheral modules to FPGA-based carrier boards. The FPIC architecture provides a direct and lightweight connection between a module's I/O resources and the FPGA, enabling designers to integrate additional functionality without the need for protocol conversion layers or complex bridging logic.

FPIC supports three module categories: FPIC ST for general-purpose digital interfaces, FPIC GT4 for 4-lane high-speed transceiver applications, and FPIC GT8 for 8-lane high-speed transceiver applications. All module types share a common mechanical framework while providing different electrical capabilities.

2. Conventions and Keywords

The following keywords are used throughout this document to indicate the level of requirement:

Keyword	Meaning
SHALL	Mandatory requirement. Compliance is required for conformance to this standard.
SHALL NOT	Prohibited. The action or condition must not occur in a conformant implementation.
SHOULD	Recommended. Deviation is permitted but must be justified and documented.
SHOULD NOT	Not recommended. Deviation is permitted but must be justified.
MAY	Permitted. The feature or behaviour is optional.

3. Introduction

3.1 Objectives

The objective of the FPIC Standard is to define a unified, high-performance, mechanically reliable, and electrically robust interface that enables modular expansion of FPGA platforms using standardised peripheral boards. FPIC establishes a common connector architecture, pin-field organisation, mechanical envelope, and electrical behaviour to ensure seamless interoperability between FPGA carrier boards and a wide range of peripheral modules.

- Support high-speed serial interfaces with data rates of **up to 10 Gb/s per differential lane**, enabling reliable operation through adaptive signal equalization.
- Support single-ended and differential I/O interfaces with signalling rates of **up to 2 Gb/s**, subject to FPGA and device capabilities.
- Utilize a compact connector and module form factor suitable for space-constrained embedded systems.
- Support both commercial and air-cooled/ruggedized implementations through common mechanical interfaces.

3.2 Overview

FPIC is a versatile connector standard designed specifically for FPGA-based platforms. It integrates user configurable I/O, differential pairs, power rails, and optional high-speed transceiver lanes into a compact and efficient form factor. The interface supports flexible voltage levels, multiple signalling standards, and modular peripheral expansion.

3.3 Normative References

The following documents are referenced normatively in this standard:

Standard	Title
IPC-2221B	Generic Standard on Printed Board Design
IPC-2141A	Controlled Impedance Circuit Boards and High-Speed Logic
PICMG 2.9	IPMI on Compact PCI
IPMI FRU ISD V1.0	Platform Management FRU Information Storage Definition
JESD22-A114	Electrostatic Discharge Sensitivity Testing — Human Body Model
IEC 60512-2	Connectors for Electronic Equipment — Tests and Measurements
CISPR 32	EMC of Multimedia Equipment — Emission Requirements
UL 94	Standard for Tests for Flammability of Plastic Materials
RoHS 2011/65/EU	Restriction of Hazardous Substances in Electrical Equipment

3.4 Glossary

Term	Definition
FPIC	FPGA Peripheral Interface Connector — standard interface between FPGA carriers and modules
FPIC ST	FPIC variant for general-purpose single-ended and differential I/O (no SERDES)
FPIC GT4	FPIC variant supporting 4 high-speed transceiver lanes plus 16 IO pairs
FPIC GT8	FPIC variant supporting 8 high-speed transceiver lanes plus 16 IO pairs
Carrier	The FPGA main board hosting FPIC ports and powering modules
Module	A peripheral board that plugs into the carrier through the FPIC connector
GT Lane	One full-duplex high-speed serial transceiver lane (TX pair + RX pair)
VIO	I/O bank supply voltage.
SERDES	Serialiser / De-serialiser - the FPGA's high-speed transceiver hard block
REF_CLK	Differential reference clock input to the FPGA SERDES quad
PG_M2C / PRSNT_M2C	Power Good and Present Detect, module to carrier — active-high signal indicating module supplies are stable
GA0, GA1	Geographic Address pins — define module slot number for I2C addressing
FRU	Field Replaceable Unit — IPMI term for a manageable hardware component
EEPROM	Non-volatile memory on the module storing identification
Ruggedized	Provides increased resistance to shock and vibration relative to commercial products.

4. FPIC Module

4.1 FPIC ST Module

4.1.1 Overview

The FPIC ST module provides general-purpose digital and mixed-signal expansion. It uses a single 80-pin QTE connector and the user I/O interface supports applications ranging from low-speed control interfaces to high-speed single-ended and differential I/O, depending on the capabilities of the FPGA device and system implementation. FPIC ST does not include SERDES lanes.

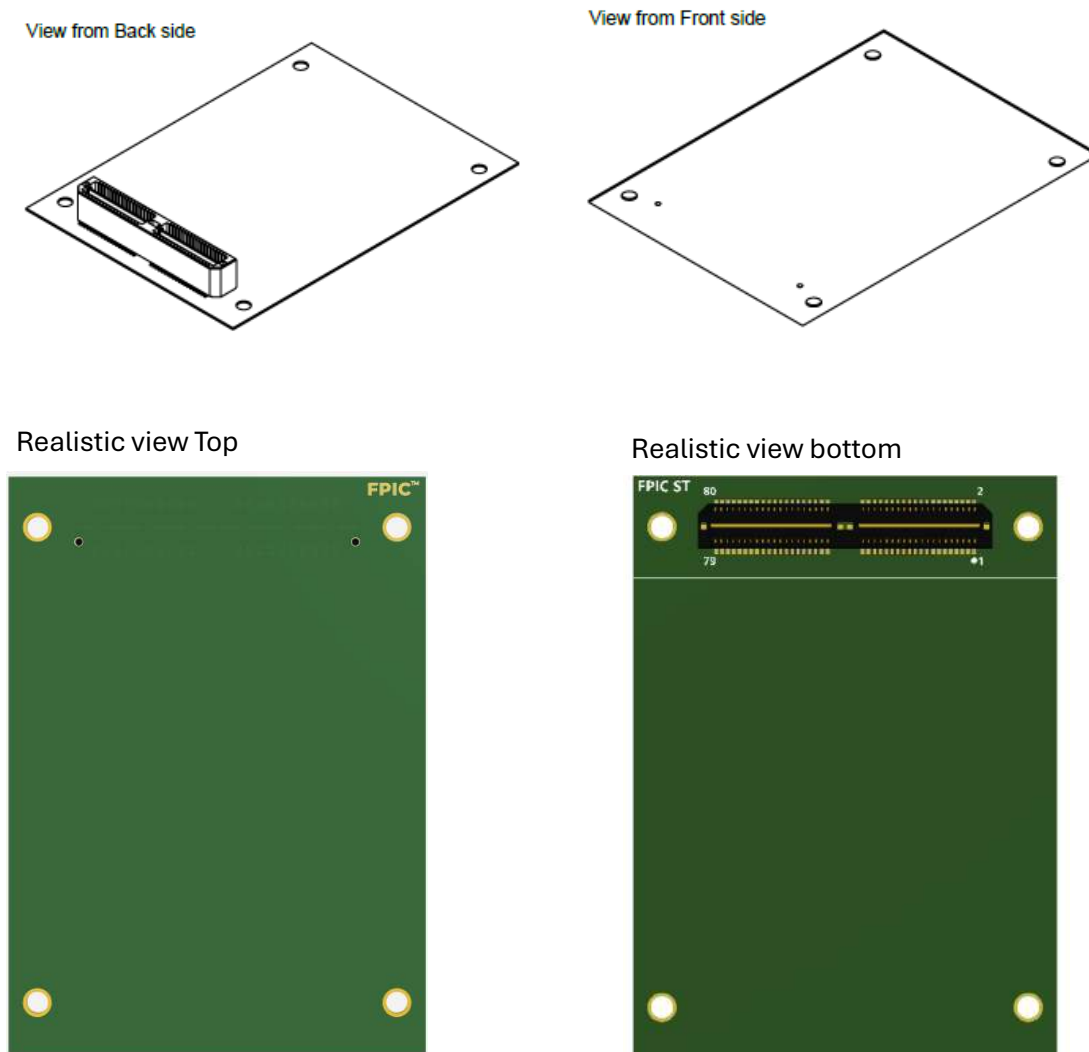


Figure 1: FPIC ST Single Module

4.1.2 FPIC ST Module Dimension

The FPIC ST module has an overall PCB dimension of **58.0mm × 80.0mm** and incorporates **four Ø3.0mm mounting holes** located **4.0mm** from the side edges and **7.0mm** from the top and bottom edges.

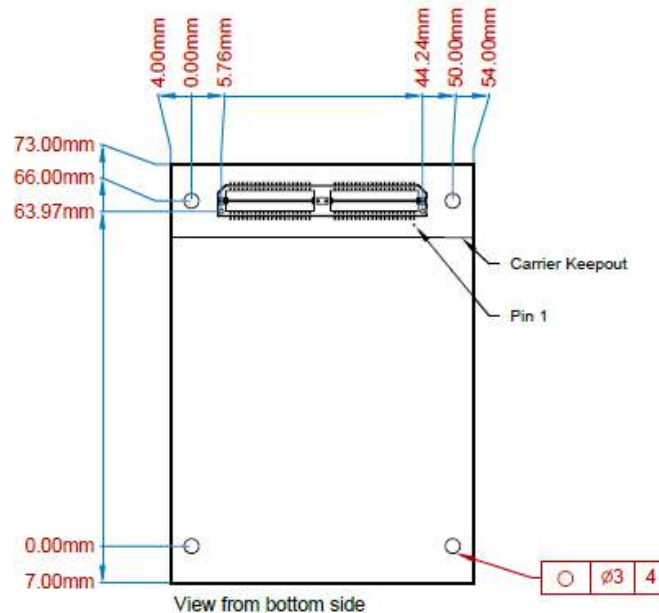


Figure 2: FPIC ST Module Dimension

4.1.3 FPIC ST Air cooled Module Dimension

The FPIC ST Air Cooled module has an overall PCB dimension of **62.0mm × 84.0mm** and incorporates **four Ø3.0mm mounting holes** located **6.0mm** from the side edges and **9.0mm** from the top and bottom edges.

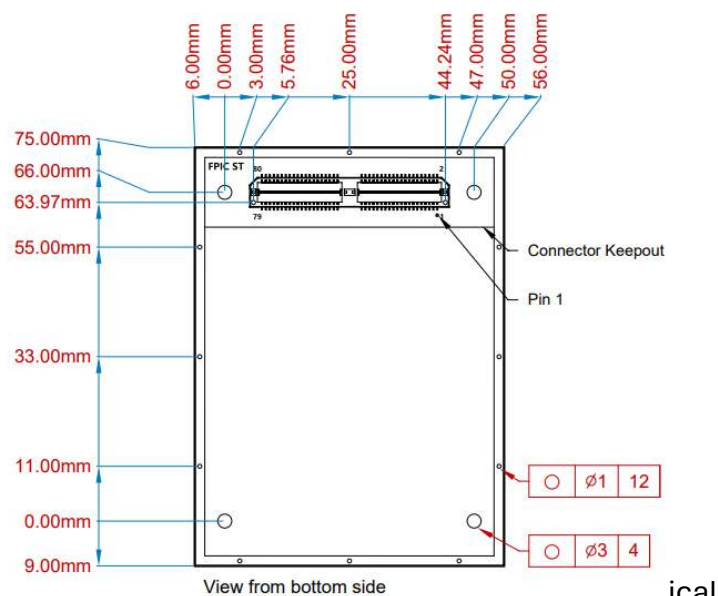


Figure 3: FPIC ST Air cooled module Dimension
NOTE: All Dimensions are in mm unless otherwise specified.

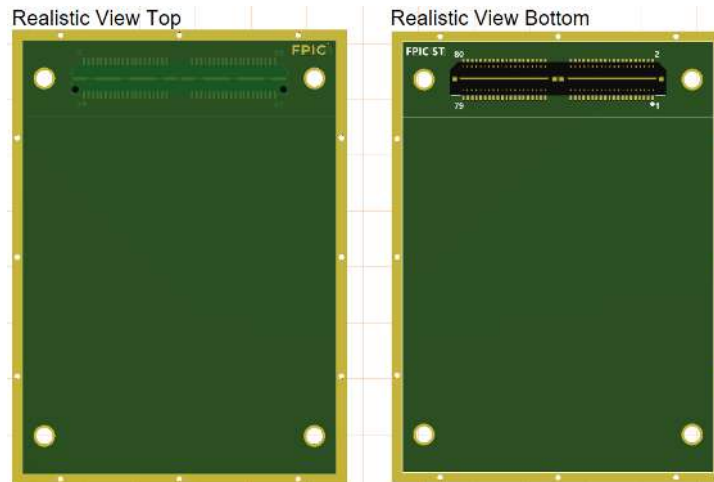


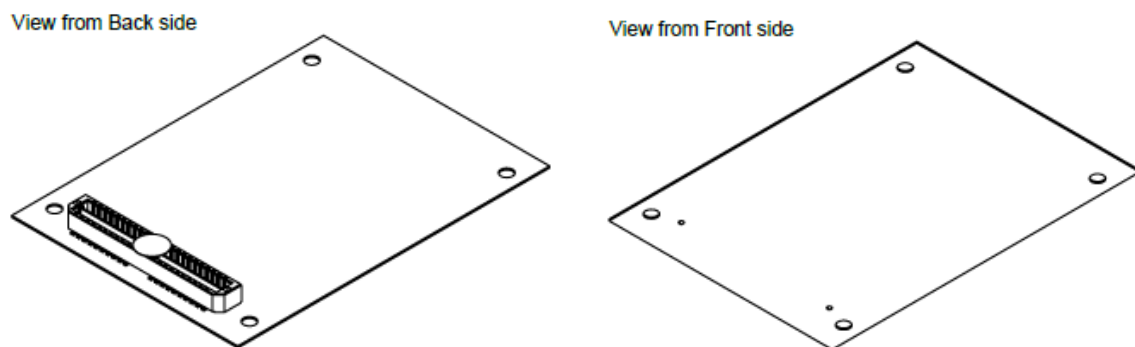
Figure 4: FPIC ST Air Cooled Module Realistic View

4.2 FPIC GT4 / FPIC GT8 Module

4.2.1 Overview

FPIC GT4 and FPIC GT8 modules are designed for high-performance applications requiring multi-gigabit transceiver links. Both variants use the same high-speed QTH connector (QTH-040-02-L-D-DP-A) and share an identical 80-pin mechanical form factor, enabling full cross-compatibility at the connector level.

FPIC GT4 implements up to 4 active transceiver lanes (GT Quad 0). FPIC GT8 implements up to 8 transceiver lanes (GT Quad 0 and GT Quad 1).



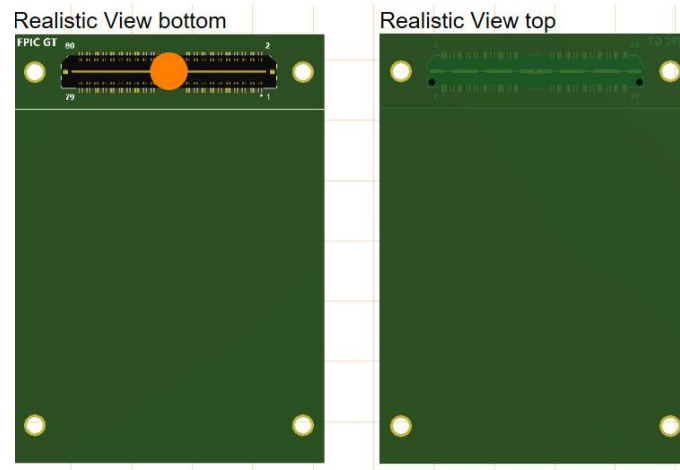


Figure 5: FPIC GT Single Module

4.2.2 FPIC GT4 & GT8 Module Dimension

The FPIC GT4 & GT8 module has an overall PCB dimension of **58.0mm × 80.0mm** and incorporates **four Ø3.0mm mounting holes** located **4.0mm** from the side edges and **7.0mm** from the top and bottom edges.

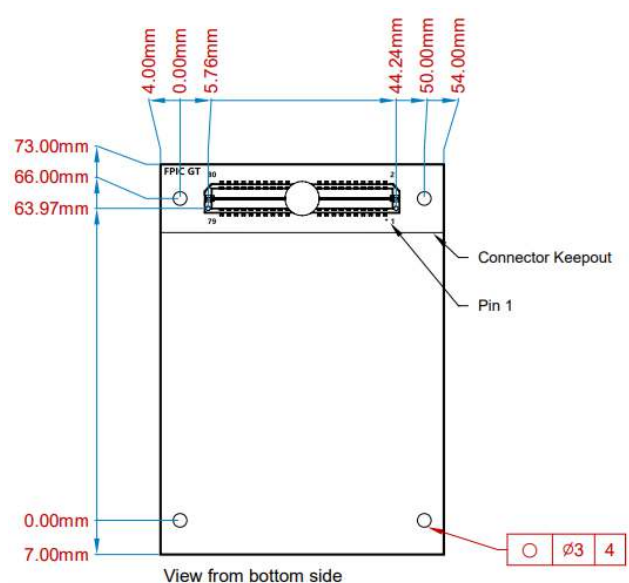


Figure 6: FPIC GT Module Dimension

4.2.3 FPIC GT4 & GT8 Air Cooled Module Dimension

The FPIC GT4 & GT8 Air Cooled module has an overall PCB dimension of **62.0mm × 84.0mm** and incorporates **four Ø3.0mm mounting holes** located **6.0mm** from the side edges and **9.0mm** from the top and bottom edges.

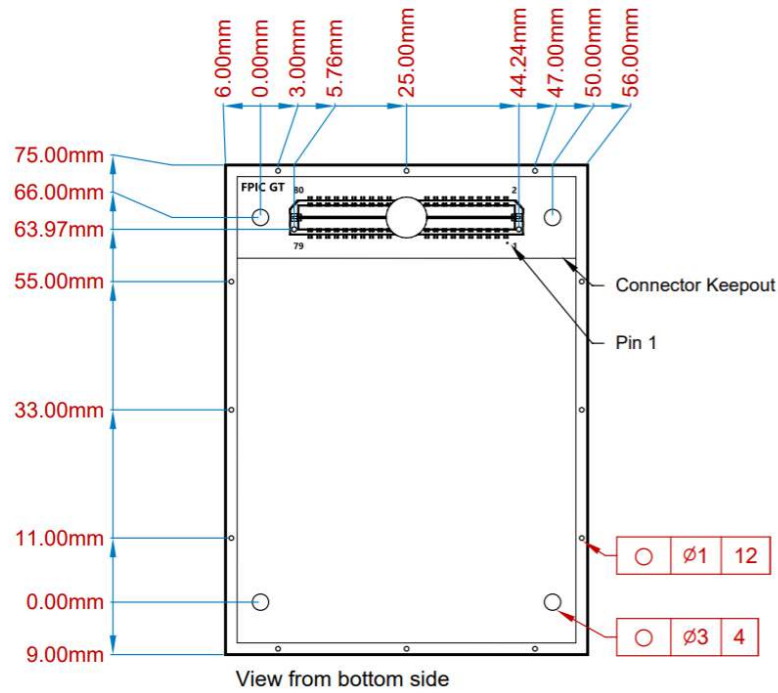


Figure 7: FPIC GT Air Cooled Module Dimension

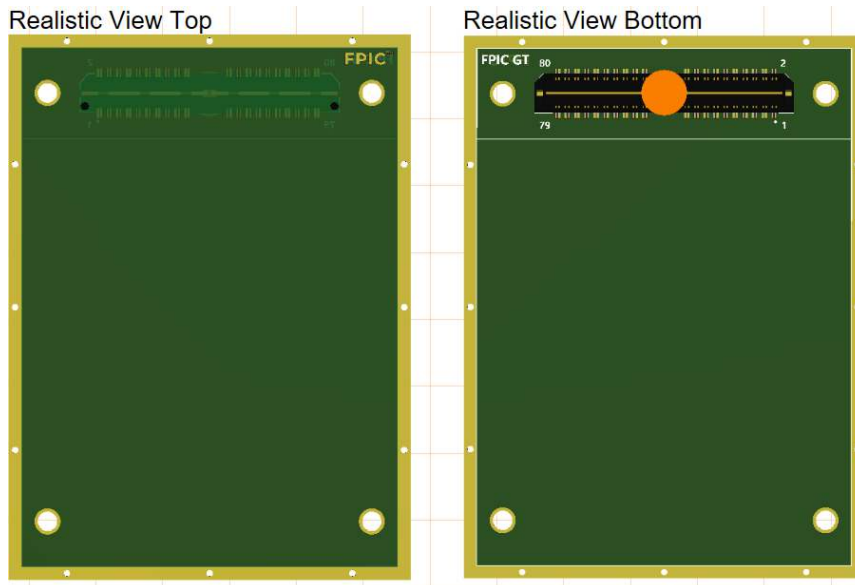


Figure 8: FPIC GT Air Cooled Module Realistic View

4.2.4 GT Lane Direction Convention

GT lane direction is defined as follows and SHALL be adhered to in all FPIC GT module and carrier designs:

Signal	Direction	Description
GT_RXx_P/N	Module → Carrier	Module transmits; carrier FPGA receives
GT_TXx_P/N	Carrier → Module	Carrier FPGA transmits; module receives
REF_CLKx_P/N	Module → Carrier	Module oscillator drives reference clock to carrier FPGA SERDES input

NOTE: TX is always named from the perspective of the carrier.

5. FPIC Carrier

The FPIC carrier is the FPGA main board that hosts one or more FPIC connector sites and supplies power, clock, and I/O resources to installed modules. The carrier SHALL implement the power sequencing, VIO Selection, and presence detection protocols defined in this standard.

5.1 FPIC Carrier Dimension

FPIC Carrier Mechanical Requirements: The dimensions of the FPIC carrier board **SHALL** be sufficient to accommodate one or more FPIC connectors, as required by the intended application. The **mechanical mounting hole locations and hole diameters SHALL match the corresponding FPIC module specification** to ensure mechanical compatibility. When an FPIC module is intended to be mounted at the **edge of the carrier PCB**, the **Region 1** dimensions **SHALL** be implemented without deviation. When the FPIC module is mounted away from the PCB edge, **both Region 1 and Region 2** dimensions **SHALL** be implemented in accordance with this specification. (Refer section 5.3 for region details)

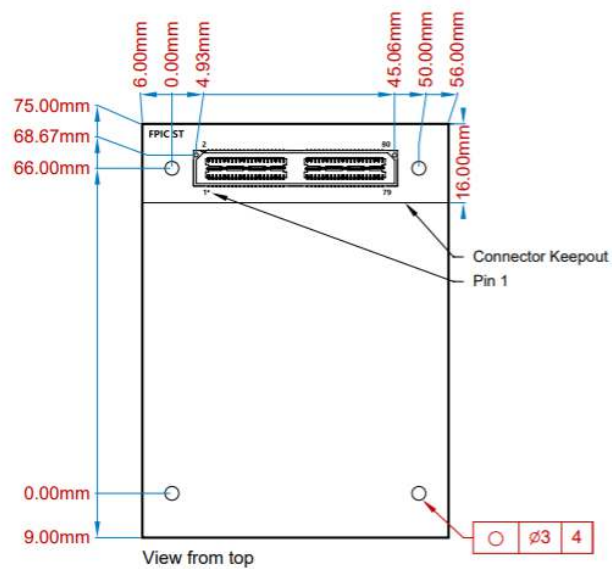


Figure 9: FPIC ST Carrier Dimension

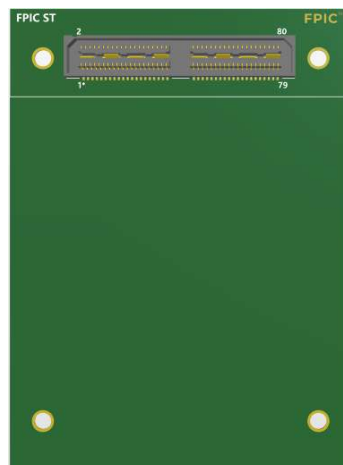


Figure 10: FPIC ST Carrier Realistic View

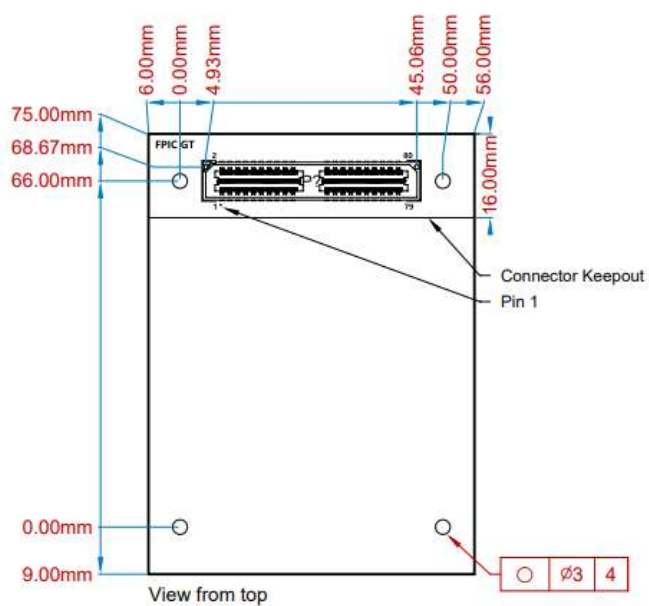


Figure 11: FPIC GT Carrier Dimension

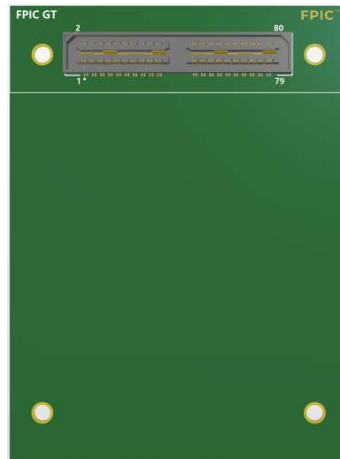


Figure 12: FPIC GT Carrier Realistic View

5.2 Multiple connector placement requirements

For designs incorporating multiple FPIC connectors, the connector-to-connector spacing SHALL meet the minimum mechanical clearance requirements specified in Figure 13 to ensure proper module installation, removal, and mechanical compatibility.

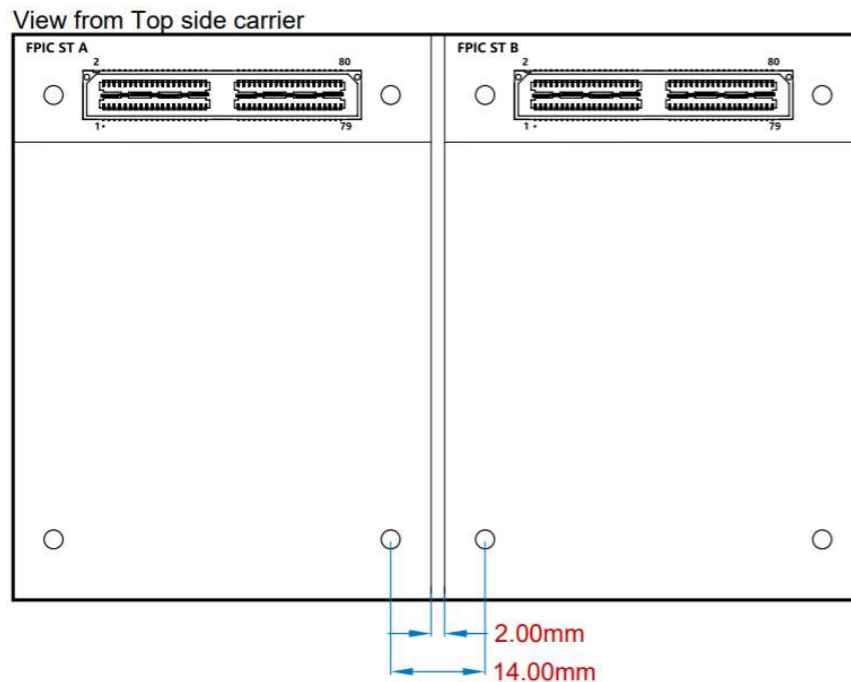


Figure 13: FPIC multiple connector placement requirement.

5.3 Component Height Envelopes

Region	Maximum Height — Commercial	Maximum Height — Air Cooled (Ruggedized)
Region 1 (connector side) — connector zone	Connector protrusion only	Connector protrusion only
Region 2 — component zone top	16mm above PCB surface	12mm above PCB surface
Region 2 — component zone bottom (Below PCB surface)	<ul style="list-style-type: none"> • 3.4mm for 5mm stacking height. • 6.5mm for 8mm stacking height. • 9.5mm for 11mm stacking height. 	<ul style="list-style-type: none"> • 3.4mm for 5mm stacking height. • 6.5mm for 8mm stacking height. • 9.5mm for 11mm stacking height.

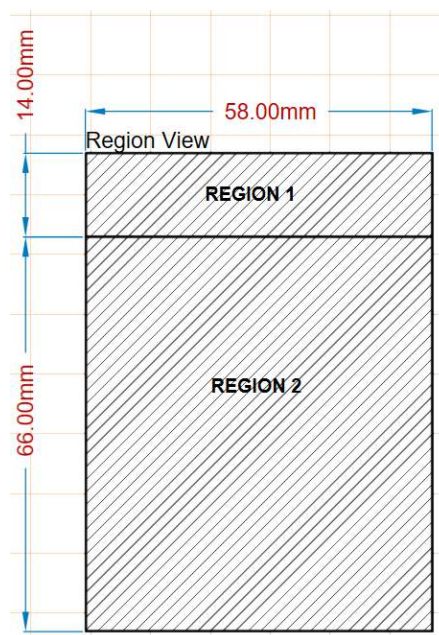


Figure 14: FPIC Module Regions

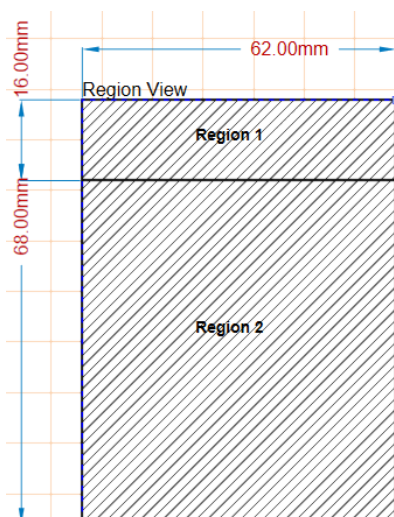


Figure 15: FPIC Air Cooled Module Regions

NOTE:

Region 2 defines the available **component placement area** on the module. The **66.0mm** dimension shown in the figure is for reference only and does not represent a fixed requirement. The actual length of region 2 may be reduced depending on the component placement and the overall module design. Designers may also implement **half-width modules** with any suitable width for Region 2, depending on component placement and overall module design. However, the **Region 1 dimensions and the specified mounting hole locations** must be maintained to ensure mechanical compatibility with the carrier.

5.4 Environmental Specifications

Parameter	Commercial Grade	Industrial / Ruggedized Grade
Operating temperature	0°C to +70°C	-40°C to +85°C
Storage temperature	-20°C to +85°C	-55°C to +125°C
PCB flammability rating	UL94 V-0	UL94 V-0
RoHS compliance	Required	Required
REACH Compliance	Required	Required

6. Connectors

6.1 FPIC ST Connectors

The table below specifies the standard connectors for **FPIC ST** modules and carrier boards. If a peripheral module requires a different connector stacking height, an appropriate connector from the list below SHALL be selected.

1. **QTE-040-01-F-D-A - stacking height 5mm.**
2. **QTE-040-03-F-D-A - stacking height 11mm.**

Attribute	Carrier (QSE-040-01-F-D-A)	Module (QTE-040-02-F-D-A)
Manufacturer	Samtec	Samtec
Positions	80	80
Pitch	0.80mm	0.80mm
Mounting	Surface mount	Surface mount
Height above board	3.25mm	7.26mm
Mated stacking height	5mm, 8mm, 11mm	8mm

Note:

- *Increasing the connector stacking height may degrade signal integrity and reduce the maximum achievable data rate. Connector selection should be based on the target interface speed and the manufacturer's performance specifications.*
- *The stacking height shall be adjusted by changing only the connector on the mezzanine module.*

6.2 FPIC GT4 / FPIC GT8 Connectors

The table below specifies the standard connectors for FPIC GT modules and carrier boards. If a peripheral module requires a different connector stacking height, an appropriate connector from the list below SHALL be selected.

1. **QTH-040-01-L-D-DP-A - stacking height 5mm.**
2. **QTH-040-03-L-D-DP-A - stacking height 11mm.**

Attribute	Carrier (QSH-040-01-L-D-DP-A)	Module (QTH-040-02-L-D-DP-A)
Manufacturer	Samtec	Samtec
Positions	80	80
Pitch	0.50mm	0.50mm
Mounting	Surface mount	Surface mount
Height above board	3.25mm	7.26mm
Mated stacking height	5mm, 8mm, 11mm	8mm

NOTE:

- *Increasing the connector stacking height may degrade signal integrity and reduce the maximum achievable data rate. Connector selection should be based on the target interface speed and the manufacturer's performance specifications.*
- *The stacking height shall be adjusted by changing only the connector on the mezzanine module.*

7. Carrier and Module Connection

FPIC modules SHALL align mechanically with the FPIC connector on the carrier. The following rules govern physical connection:

1. Figure 15 shows the recommended placement of the carrier connector along the edge of the PCB.
2. Figure 16 shows the fully assembled mechanical interface between the FPIC module and the carrier board.

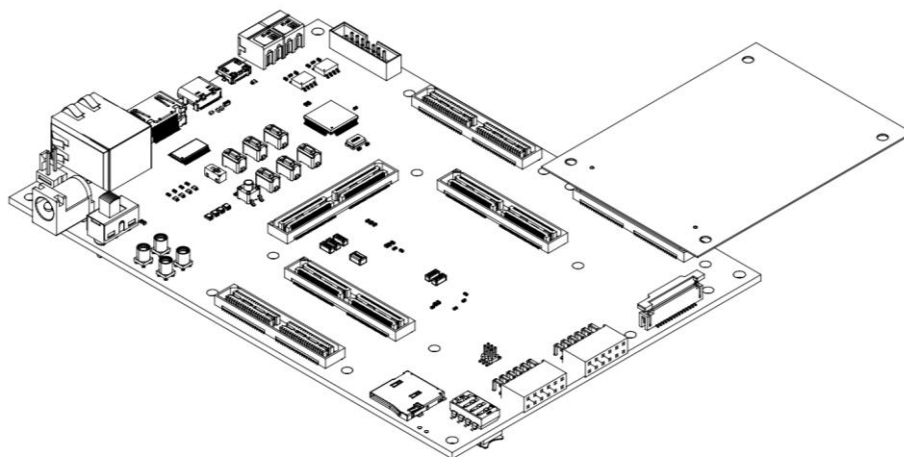


Figure 16: FPIC carrier and module Placement (PCB Edge)

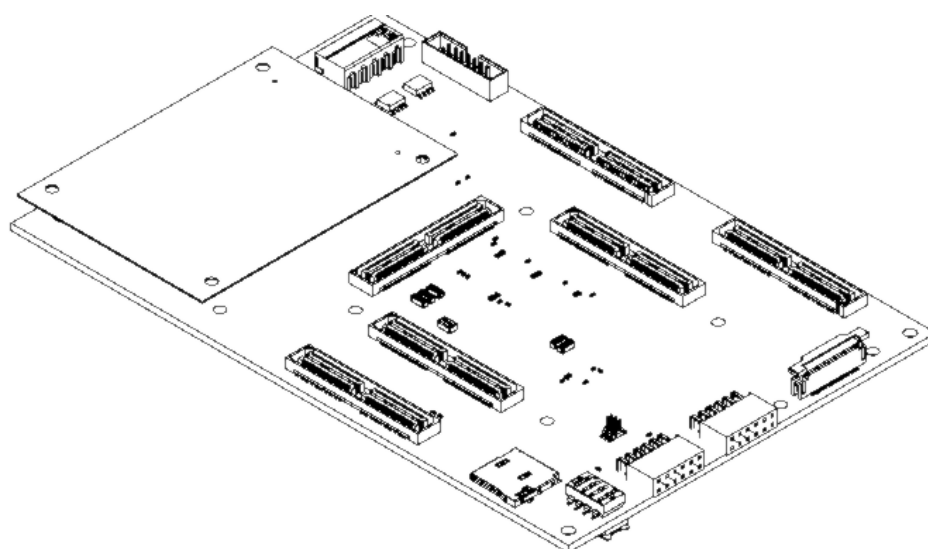


Figure 17: FPIC carrier and module Placement (Non-PCB Edge)



Figure 18: FPIC Module and Carrier Alignment

R7.1
SHALL

The carrier SHALL monitor PRSNT_M2C.

R7.2
SHALL

The module SHALL assert PG_M2C within 200ms of the 3.3V rail reaching its nominal voltage.

R7.3 SHALL	The carrier SHALL tri-state all FPIC IO pins within 200ms of PG_M2C deasserting.
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8. FPIC Pinouts and Pin Definition

8.1 Colour Key

Colour	Signal Group
Blue background	GT TX transceiver lanes (carrier → module)
Green background	GT RX transceiver lanes (module → carrier)
Amber background	Reference clock pairs
Purple background	User IO and clock-capable IO pairs
Yellow background	Power rails (5V, 3.3V, VIO, GND)
Red background	Control and management signals
Light grey	Reserved (NC / RES)

8.2 FPIC ST Connector Pin Mapping

The FPIC ST connector provides 24 differential IO pairs (IO0–IO23), 8 clock-capable pairs (CLK0–CLK7), power, ground, and management signals. No **GT** lanes are present.

Pin			Pin
5V	1	2	PG_M2C/PRSNT_M2C
GND	3	4	GND
IO0_P/CLK0_P	5	6	IO1_P/CLK1_P
IO0_N/CLK0_N	7	8	IO1_N/CLK1_N
IO2_P	9	10	IO3_P
IO2_N	11	12	IO3_N
GND	13	14	GND
IO4_P	15	16	IO5_P
IO4_N	17	18	IO5_N
IO6_P	19	20	IO7_P
IO6_N	21	22	IO7_N
GND	23	24	GND
IO8_P/CLK2_P	25	26	IO9_P/CLK3_P
IO8_N/CLK2_N	27	28	IO9_N/CLK3_N

IO10_P	29	30	IO11_P
IO10_N	31	32	IO11_N
GND	33	34	GND
IO12_P/CLK4_P	35	36	IO13_P/CLK5_P
IO12_N/CLK4_N	37	38	IO13_N/CLK5_N
IO14_P	39	40	IO15_P
IO14_N	41	42	IO15_N
GND	43	44	GND
IO16_P	45	46	IO17_P
IO16_N	47	48	IO17_N
IO18_P	49	50	IO19_P
IO18_N	51	52	IO19_N
GND	53	54	GND
IO20_P/CLK6_P	55	56	IO21_P/CLK7_P
IO20_N/CLK6_N	57	58	IO21_N/CLK7_N
IO22_P	59	60	IO23_P
IO22_N	61	62	IO23_N
GND	63	64	GND
RES	65	66	RES
RES	67	68	RES
GA0	69	70	GA1
VIO1	71	72	SCL
VIO2	73	74	SDA
GND	75	76	GND
3.3V	77	78	3.3V
3.3V	79	80	3.3V

8.3 FPIC GT4 Connector Pin Mapping

The FPIC GT4 connector provides 4 GT transceiver lanes (GT **Quad 0**, lanes **0–3**), one reference clock pair (**REF_CLK0**), 16 IO differential pairs, and management signals. Pins 18–36 (even) and 21–35 (odd) are NC and reserved for GT8 use — they SHALL NOT be connected on GT4 modules.

Pin			Pin
GT_TX0_P	1	2	GT_RX0_P
GT_TX0_N	3	4	GT_RX0_N
GT_TX1_P	5	6	GT_RX1_P
GT_TX1_N	7	8	GT_RX1_N
GT_TX2_P	9	10	GT_RX2_P
GT_TX2_N	11	12	GT_RX2_N
GT_TX3_P	13	14	GT_RX3_P
GT_TX3_N	15	16	GT_RX3_N

REF_CLK0_P	17	18	NC
REF_CLK0_N	19	20	NC
NC	21	22	NC
NC	23	24	NC
NC	25	26	NC
NC	27	28	NC
NC	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	NC
IO0_P/CLK0_P	37	38	IO1_P/CLK1_P
IO0_N/CLK0_N	39	40	IO1_N/CLK1_N
IO2_P	41	42	IO3_P
IO2_N	43	44	IO3_N
IO4_P	45	46	IO5_P
IO4_N	47	48	IO5_N
IO6_P	49	50	IO7_P
IO6_N	51	52	IO7_N
IO8_P/CLK2_P	53	54	IO9_P/CLK3_P
IO8_N/CLK2_N	55	56	IO9_N/CLK3_N
IO10_P	57	58	IO11_P
IO10_N	59	60	IO11_N
IO12_P	61	62	IO13_P
IO12_N	63	64	IO13_N
IO14_P	65	66	IO15_P
IO14_N	67	68	IO15_N
RES	69	70	GA0
PG_M2C/ PRSNT_M2C	71	72	GA1
VIO1	73	74	SCL
VIO2	75	76	SDA
5V	77	78	3.3V
5V	79	80	3.3V

8.4 FPIC GT8 Connector Pin Mapping

The FPIC GT8 connector provides 8 GT transceiver lanes across two quads (Quad 0: lanes 0–3, Quad 1: lanes 4–7), two independent reference clock pairs (**REF_CLK0** for Quad 0, **REF_CLK1** for Quad 1), 16 IO differential pairs, and management signals.

Pin			Pin
GT_TX0_P	1	2	GT_RX0_P
GT_TX0_N	3	4	GT_RX0_N

GT_TX1_P	5	6	GT_RX1_P
GT_TX1_N	7	8	GT_RX1_N
GT_TX2_P	9	10	GT_RX2_P
GT_TX2_N	11	12	GT_RX2_N
GT_TX3_P	13	14	GT_RX3_P
GT_TX3_N	15	16	GT_RX3_N
REF_CLK0_P	17	18	REF_CLK1_P
REF_CLK0_N	19	20	REF_CLK1_N
GT_TX4_P	21	22	GT_RX4_P
GT_TX4_N	23	24	GT_RX4_N
GT_TX5_P	25	26	GT_RX5_P
GT_TX5_N	27	28	GT_RX5_N
GT_TX6_P	29	30	GT_RX6_P
GT_TX6_N	31	32	GT_RX6_N
GT_TX7_P	33	34	GT_RX7_P
GT_TX7_N	35	36	GT_RX7_N
IO0_P/CLK0_P	37	38	IO1_P/CLK1_P
IO0_N/CLK0_N	39	40	IO1_N/CLK1_N
IO2_P	41	42	IO3_P
IO2_N	43	44	IO3_N
IO4_P	45	46	IO5_P
IO4_N	47	48	IO5_N
IO6_P	49	50	IO7_P
IO6_N	51	52	IO7_N
IO8_P/CLK2_P	53	54	IO9_P/CLK3_P
IO8_N/CLK2_N	55	56	IO9_N/CLK3_N
IO10_P	57	58	IO11_P
IO10_N	59	60	IO11_N
IO12_P	61	62	IO13_P
IO12_N	63	64	IO13_N
IO14_P	65	66	IO15_P
IO14_N	67	68	IO15_N
RES	69	70	GA0
PG_M2C/ PRSNT_M2C	71	72	GA1
VIO1	73	74	SCL
VIO2	75	76	SDA
5V	77	78	3.3V
5V	79	80	3.3V

9. Pin Definitions

9.1 User I/O Pins

The FPIC interface includes user-defined I/O pins that may operate as single-ended signals or differential pairs. I/O pin voltage levels are determined by the VIO rail.

Parameter	Specification	Notes
Supported voltage range (VIO)	1.2 V to 3.3V	Set by carrier
Signal tolerance	VIO $\pm$ 200 mV	Neither side SHALL exceed this
Differential impedance	100 Ω $\pm$ 10%	For LVDS operation
I/O standards supported	LVC MOS, LV TTL, SSTL, HSTL, LVDS	FPGA bank dependent
ST-FPIC IO count	48 SE / 24 differential pairs	IO0–IO23
GT-FPIC IO count	32 SE / 16 differential pairs	IO0–IO15
R9.1 SHALL NOT	IO pins SHALL NOT be driven outside the VIO $\pm$ 200 mV range by either the carrier or the module.	
R9.2 SHALL	Unused IO pins SHALL be pulled to a defined logic level (pull-up or pull-down). Floating IO pins are prohibited.	

9.2 FPIC ST Pin Definitions

9.2.1 User I/O Signals

IO [0..23] P, IO [0..23] N – These differential signal pairs provide the primary user-defined I/O interface between the FPIC ST module and the carrier. Each differential pair may be used as either a differential signal pair or as two independent single-ended I/O signals, subject to the FPGA I/O bank capabilities and the selected I/O standard.

9.2.2 I/O Bank Assignment Recommendation

To ensure compatibility across FPGA families and to preserve the clock-capable I/O relationships, the FPIC ST user I/O signals should be assigned to FPGA I/O banks as follows:

R9.3 SHOULD	The IO0_P/N through IO11_P/N differential pairs should be routed to a single FPGA I/O bank. (BANK A)
R9.4 SHOULD	The IO12_P/N through IO23_P/N differential pairs should be routed to a second FPGA I/O bank. (BANK B)
R9.5 SHALL	SHALL FPGA devices that provide a single I/O bank with sufficient user I/O resources may route IO0_P/N through IO23_P/N to the same FPGA I/O bank.
R9.6 SHALL NOT	Partial assignment of the IO12–IO23 group before completing the IO0–IO11 group, or intermixing signals between the two FPGA I/O banks, SHALL NOT be permitted.

9.2.3 Clock-Capable I/O Signals and Associated I/O Signals

Clock-capable IO pairs are physically routed to FPGA global or regional clock-capable inputs. They support reference clocks, source-synchronous interfaces, and timing-critical signals.

Variant	Mandatory CLK pairs	Optional CLK pairs	Total
FPIC ST	CLK0, CLK1, CLK4, CLK5	CLK2, CLK3, CLK6, CLK7	8

Recommended Clock-Capable I/O Signal Association:

Primary CC Signal	Preferred User I/O Signals	Secondary CC Signal
IO0_P/N	IO1 – IO11	IO1_P/N
IO12_P/N	IO12 – IO23	IO13_P/N

Recommendation: For carrier board designs using UltraScale or UltraScale+ FPGAs, where available, it is recommended to assign the GC_QBC - capable pins to **IO0_P/CLK0_P** and **IO0_N/CLK0_N** to support clock-related functionality. This recommendation is optional.

9.2.4 Power Rails

- **5V** – Main power supply provided by the carrier to the FPIC ST module, supporting up to **2 A per connector pin**.
- **3.3V** – Auxiliary 3.3V power supplied by the carrier for module circuitry, supporting up to **2 A per connector pin**.
- **GND** – Common ground reference shared between the carrier and the module.

9.2.5 PG_M2C/PRSNT_M2C

PG_M2C / PRSNT_M2C is a multifunction signal used for both **module detection** and **power-good indication**. During module insertion, it is used by the carrier to detect the presence of the module. After all required power rails on the module have reached their valid operating levels, the module drives this signal **High** to indicate that power is stable, and the module is ready for operation.

R9.7 SHALL	The carrier SHALL provide a 10 kΩ ±10% pull-down resistor on the PG_M2C / PRSNT_M2C signal. The module SHALL provide a 1 kΩ ±10% pull-up to 3.3V. After all required module power rails have reached their valid operating levels, the module SHALL actively drive the PG_M2C / PRSNT_M2C signal High to indicate a Power Good condition.
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9.2.6 Geographic Address Pins (GA0, GA1)

GA pins identify the physical slot position of the installed FPIC module and determine the module's I2C address. See §10.2 for the I2C address formula.

GA1	GA0	Slot / Port ID	I2C EEPROM Address
0	0	Slot 0	0x50
0	1	Slot 1	0x51
1	0	Slot 2	0x52
1	1	Slot 3	0x53
R9.8 SHALL	The carrier SHALL pull the GA0 and GA1 signals to defined logic levels before module power-up. The module SHALL connect the GA0 and GA1 signals to the A0 and A1 address pins, respectively, of the recommended EEPROM. The GA0 and GA1 signals SHALL NOT be left floating.		

9.2.7 SCL / SDA — I2C Management

Parameter	Specification
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Pull-up resistors	4.7k Ω on the carrier side (SHALL NOT be placed on module)
I/O voltage domain	Fixed 3.3V on carrier
Voltage tolerance	3.3V $\pm$ 300 mV
Minimum speed	Standard-mode 100kHz
Recommended speed	Fast-mode 400kHz
SDA function	Bidirectional data line
SCL function	Clock line (carrier is master)

9.2.8 VIO Reference Voltages

The **VIO1** and **VIO2** signals define the reference I/O bank voltage supplied by the carrier to the FPIC ST module. These voltages determine the operating voltage of the associated user I/O signals and shall be compatible with the I/O standards supported by both the FPGA and the module.

VIO1 – Reference I/O bank voltage associated with the **IO0_P/N through IO11_P/N** differential I/O group.

VIO2 – Reference I/O bank voltage associated with the **IO12_P/N through IO23_P/N** differential I/O group.

NOTE:

*If all 24 differential I/O pairs (IO0–IO23) are implemented within a single FPGA I/O bank, either **VIO1** or **VIO2** may be connected, provided the selected supply voltage matches the FPGA I/O bank reference voltage.*

9.3 FPIC GT4 / GT8 Pin Definitions

9.3.1 High-Speed Transceiver Signals

GT_TX[0..7]_P, GT_TX[0..7]_N – Differential high-speed transmitter pairs from the FPGA to the FPIC GT connector. These signals are intended for high-speed serial interfaces such as Ex: PCI Express, Ethernet, JESD204, Aurora and other FPGA transceiver-based protocols.

GT_RX[0..7]_P, GT_RX[0..7]_N – Differential high-speed receiver pairs from the FPIC GT connector to the FPGA. These signals shall be routed as controlled-impedance differential pairs in accordance with the Peripheral design guidelines.

REF_CLK0_P/N – Differential reference clock pair associated with **GT Quad 0**.

REF_CLK1_P/N – Differential reference clock pair associated with **GT Quad 1**.

The reference clock pairs provide low-jitter clock sources for the FPGA transceiver quads and should be connected to dedicated transceiver reference clock inputs.

Note: The **FPIC GT8** connector provides **eight transmit and eight receive differential transceiver pairs**. The **FPIC GT4** connector provides only **GT Quad 0**. The signals corresponding to **GT Quad 1**, including **REF_CLK1**, are **not connected** in the **FPIC GT4** connector.

9.3.2 I/O Bank Assignment Recommendation

To ensure compatibility across FPGA families and to preserve the clock-capable I/O relationships, the FPIC GT user I/O signals should be assigned to FPGA I/O banks as follows:

R9.9 SHOULD	The IO0_P/N through IO7_P/N differential pairs should be routed to a single FPGA I/O bank.
R9.10 SHOULD	The IO8_P/N through IO15_P/N differential pairs should be routed to a second FPGA I/O bank.
R9.11 SHALL	SHALL FPGA devices that provide a single I/O bank with sufficient user I/O resources may route IO0_P/N through IO15_P/N to the same FPGA I/O bank.
R9.12 SHALL NOT	Partial assignment of the IO8–IO15 group before completing the IO0–IO7 group, or intermixing signals between the two FPGA I/O banks, SHALL NOT be permitted.

9.3.3 Clock-Capable I/O Signals and Associated I/O Signals

Clock-capable IO pairs are physically routed to FPGA global or regional clock-capable inputs. They support reference clocks, source-synchronous interfaces, and timing-critical signals.

Variant	Mandatory CLK pairs	Optional CLK pairs	Total
FPIC GT4	CLK0, CLK1, CLK2, CLK3	—	4 (all mandatory)
FPIC GT8	CLK0, CLK1, CLK2, CLK3	—	4 (all mandatory)

Recommended Clock-Capable I/O Signal Association:

Primary CC Signal	Preferred User I/O Signals	Secondary CC Signal
IO0_P/N	IO1 – IO7	IO1_P/N
IO8_P/N	IO8 – IO15	IO9_P/N

9.3.4 GT Transceiver Data Pins

GT transceiver pins carry high-speed serial data between the module and carrier FPGA SERDES resources. They SHALL NOT be repurposed as GPIO or used for low-speed logic.

Parameter	Specification
Lane direction — TX	GT_TXx_P/N: carrier → module (carrier drives)
Lane direction — RX	GT_RXx_P/N: module → carrier (module drives)
Differential impedance	100Ω ± 10% end-to-end
P/N polarity	SHALL be preserved. Inversion only if compensated in FPGA SERDES
AC coupling	100nF 0402 SHALL be placed on TX pairs within 5mm of connector
Unused lanes	SHALL be SERDES-terminated or powered down. SHALL NOT float
Supported transceivers	GTR, GTH, GTX, GTY, GTP (Xilinx/AMD); GX, GT (Intel/Altera)

9.3.5 Reference Clock Pins (REF_CLK0, REF_CLK1)

Reference clock pairs supply the timing reference for FPGA SERDES quads. REF_CLK0 serves GT Quad 0 (lanes 0–3). REF_CLK1 serves GT Quad 1 (lanes 4–7) and is available on FPIC GT8 only.

Parameter	Specification
Direction	Module → carrier (module oscillator drives FPGA REFCLK input)
Oscillator location	SHALL reside on the FPIC module

Impedance	100Ω ± 10% differential
Polarity	SHALL be preserved (P/N)
Unused REF_CLK pairs	SHALL remain electrically safe — no floating differential pairs
Repurposing	REF_CLK pins SHALL NOT be used for user I/O or low-speed signals

9.3.6 Power Rails

- **5V** – Main power supply provided by the carrier to the FPIC GT module, supporting up to **2 A per connector pin**.
- **3.3V** – Auxiliary 3.3V power supplied by the carrier for module circuitry, supporting up to **2 A per connector pin**.
- **GND** – Common ground reference shared between the carrier and the module.

9.3.7 PG_M2C/PRSNT_M2C

PG_M2C / PRSNT_M2C is a multifunction signal used for both **module detection** and **power-good indication**. During module insertion, it is used by the carrier to detect the presence of the module. After all required power rails on the module have reached their valid operating levels, the module drives this signal **High** to indicate that power is stable, and the module is ready for operation.

R9.13 SHALL	The carrier SHALL provide a 10kΩ ±10% pull-down resistor on the PG_M2C / PRSNT_M2C signal. The module SHALL provide a 1kΩ ±10% pull-up resistor to 3.3V. After all required module power rails have reached their valid operating levels, the module SHALL actively drive the PG_M2C / PRSNT_M2C signal High to indicate a Power Good condition.
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9.3.8 Geographic Address Pins (GA0, GA1)

GA pins identify the physical slot position of the installed FPIC module and determine the module's I2C address. See §10.2 for the I2C address formula.

GA1	GA0	Slot / Port ID	I2C EEPROM Address
0	0	Slot 0	0x50
0	1	Slot 1	0x51

1	0	Slot 2	0x52
1	1	Slot 3	0x53
R9.14 SHALL	The carrier SHALL pull GA0 and GA1 to defined logic levels before module power-up. GA pins SHALL NOT float.		

9.3.9 SCL / SDA — I2C Management

Parameter	Specification
Pull-up resistors	4.7kΩ on the carrier side (SHALL NOT be placed on module)
I/O voltage domain	Fixed 3.3V on carrier
Voltage tolerance	3.3V ± 300mV
Minimum speed	Standard-mode 100kHz
Recommended speed	Fast mode 400kHz
SDA function	Bidirectional data line
SCL function	Clock line (carrier is master)

9.3.10 VIO Reference Voltages

The **VIO1** and **VIO2** signals define the reference I/O bank voltage supplied by the carrier to the FPIC GT module. These voltages determine the operating voltage of the associated user I/O signals and shall be compatible with the I/O standards supported by both the FPGA and the module.

VIO1 – Reference I/O bank voltage associated with the **IO0_P/N through IO7_P/N** differential I/O group.

VIO2 – Reference I/O bank voltage associated with the **IO8_P/N through IO15_P/N** differential I/O group.

NOTE:

*If all **16 differential I/O pairs** are assigned to a single FPGA I/O bank, **VIO1** and **VIO2** shall be connected to the same I/O bank supply voltage to maintain a common reference voltage for all user I/O signals.*

10. Module Management — EEPROM & I2C

10.1 EEPROM Requirements

Every FPIC module SHALL contain a non-volatile EEPROM accessible via the I2C bus on SDA/SCL. The EEPROM SHALL store module identification and power configuration data in the format defined below.

R10.1 SHALL	Recommended EEPROM: Microchip 24AA025E48 or 24AA025E64 in the SOIC package. The A2 address pin shall be connected to Logic 0 (GND) .
R10.2 SHALL	Loss of EEPROM content SHALL NOT occur during normal power cycling.

10.2 I2C Address Assignment

The FPIC module EEPROM SHALL respond at a 7-bit I2C address determined by the GA0 and GA1 pins as follows:

Address = 0b1010_0_GA1_GA0

Range: 0x50 (Slot 0) to 0x53 (Slot 3)

R10.3 SHALL NOT	I2C devices on the module SHALL NOT use addresses 0x50–0x53 for any purpose other than the FPIC EEPROM.
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11. Electrical Requirements

11.1 Signal Integrity Specifications

Parameter	GT Lanes	Differential IO Pairs	IO Pairs (LVCMOS)
Impedance	100Ω ± 10%	100Ω ± 10%	50Ω ± 10%
Intra-pair skew (max)	5ps	20ps	N/A
Inter-pair skew (max)	20ps	100ps	N/A
Max connector stub length	5mm	10mm	10mm
Max vias per lane	1 (0 preferred)	2	4
Reference plane requirement	Solid GND plane immediately below	Solid GND plane immediately below	Solid GND plane
Trace separation (min)	3× trace width	3× trace width	2× trace width

11.2 AC Coupling

R11.1 SHALL	Where required by the specific transceiver protocol or peripheral interface, 100nF $\pm 1\%$ (0402) AC-coupling capacitors SHALL be placed on all GT_TX differential lanes on the module side, as close as practical to the FPIC GT connector.
R11.2 SHALL	AC coupling capacitors for GT_RX lanes SHALL be placed on the carrier side, as close as practical to the FPIC GT connector.

11.3 VIO Negotiation Protocol

Step	Action	Performed by
1	Assert PRSNT_M2C (module installed)	Module
2	Set VIO1 and VIO2 within the module's stated range.	Carrier
3	Enable VIO1 and VIO2 rails	Carrier
4	Assert PG_M2C when all module supplies are stable	Module
5	Enable FPGA IO banks and begin normal operation	Carrier

11.4 ESD Protection

R11.3 SHALL	All FPIC IO pins SHALL tolerate HBM ESD events of ± 2 kV minimum per JESD22-A114.
R11.4 SHALL	All front-panel I/O connectors on FPIC modules (SFP+, QSFP, RJ45, SMA etc.) SHALL include ESD protection devices rated to ± 15 kV HBM.

11.5 Power Sequencing (optional)

The following power-up sequence SHALL be observed:

Order	Event	Timing
1	3.3V and 5V rails enabled by carrier	$t = 0$
2	Carrier reads EEPROM via I2C	After PRSNT_M2C asserted

3	Module asserts PG_M2C	Within 200ms of 3.3V reaching nominal
4	Carrier enables FPGA IO banks	After PG_M2C asserted
5	Module SERDES locked, normal operation	After FPGA configuration complete

12. PCB Design Rules

12.1 Differential Pair Layout Rules

R12.1 SHALL	GT lane differential pairs SHALL be routed with $100\Omega \pm 10\%$ impedances, with a continuous solid GND reference plane directly beneath the signal layer.
R12.2 SHALL	Intra-pair length mismatch SHALL NOT exceed 0.5mm for GT lanes and 2.0mm for IO pairs.
R12.3 SHALL NOT	GT lane routing SHALL NOT cross splits in the GND reference plane.
R12.4 SHOULD	GT lanes should be routed with the minimum number of vias.
R12.5 SHALL	Maintain adequate spacing between adjacent differential pairs to minimize crosstalk. A spacing of 3× the trace width is recommended where practical.

12.2 EMC Design Guidance (Informative)

The following guidance is informative and not mandatory, but is strongly recommended for FPIC modules used in end products subject to EMC certification:

Recommendation	Detail
Ground stitching vias	Place GND stitching vias around PCB perimeter at spacing $\leq \lambda/20$ at maximum operating frequency
Decoupling capacitors	Place one 100nF 0402 X7R capacitor per power pin (5V, 3.3V, VIO), within 2mm of each pin
Guard traces	Route GND guard traces on all 4 PCB edges adjacent to signal traces

Reference standards	CISPR 32, FCC Part 15 Class B
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13. Compatibility Matrix

The following matrix defines the compatibility between FPIC module and carrier variants. All FPIC variants use the same PCB outline (58.00mm × 80.00mm) and mounting hole pattern.

Module \ Carrier	FPIC ST Carrier	FPIC GT4 Carrier	FPIC GT8 Carrier
FPIC ST Module	✓ Full — all IO and power signals functional	✗ Incompatible	✗ Incompatible
FPIC GT4 Module	✗ Incompatible	✓ Full — lanes 0–3 and REF_CLK0 fully functional	✓ Partial — lanes 0–3 and REF_CLK0 functional; lanes 4–7 NC on module
FPIC GT8 Module	✗ Incompatible	✓ Partial — lanes 0–3 active.	✓ Full — all 8 lanes and both REF_CLKs functional

14. Compliance Checklist

This checklist summarises the mandatory (SHALL) requirements of this standard. Manufacturers of FPIC compliant modules and carriers SHALL verify each item before claiming conformance.

Rule ID	Requirement Summary	Applies to	Module ✓	Carrier ✓
R7.1	Carrier monitors PRSNT_M2C	Carrier	—	☐
R7.2	Module asserts PG_M2C within 200ms of 3.3V nominal	Module	☐	—
R7.3	Carrier tri-states IO within 200ms of PG_M2C deasserts	Carrier	—	☐
R9.1	IO pins not driven outside VIO ± 200 mV	Both	☐	☐
R9.2	Unused IO pins not left floating	Module	☐	—

R9.3	The IO0_P/N through IO11_P/N differential pairs should be routed to a single FPGA I/O bank. (BANK A)	Carrier	—	☐
R9.4	The IO12_P/N through IO23_P/N differential pairs should be routed to a second FPGA I/O bank. (BANK B)	Carrier	—	☐
R9.5	FPGA devices that provide a single I/O bank with sufficient user I/O resources may route IO0_P/N through IO23_P/N to the same FPGA I/O bank	Carrier	—	☐
R9.6	Partial assignment of the IO12–IO23 group before completing the IO0–IO11 group, or intermixing signals between the two FPGA I/O banks, SHALL NOT be permitted.	Carrier	—	☐
R9.7	The carrier SHALL provide a 10 k Ω $\pm$ 10% pull-down resistor on the PG_M2C / PRSNT_M2C signal. The module SHALL provide a 1 k Ω $\pm$ 10% pull-up to 3.3V.	Both	☐	☐
R9.8	The carrier SHALL pull GA0 and GA1 to defined logic levels before module power-up. GA pins SHALL NOT float.	Carrier	—	☐
R9.9	The IO0_P/N through IO7_P/N differential pairs should be routed to a single FPGA I/O bank.	Carrier	—	☐
R9.10	The IO8_P/N through IO15_P/N differential pairs should be routed to a second FPGA I/O bank.	Carrier	—	☐
R9.11	FPGA devices that provide a single I/O bank with sufficient user I/O resources may route IO0_P/N through IO15_P/N to the same FPGA I/O bank.	Carrier	—	☐
R9.12	Partial assignment of the IO8–IO15 group before completing the IO0–IO7 group, or intermixing signals between the two FPGA I/O banks, SHALL NOT be permitted.	Carrier	—	☐

R9.13	The carrier SHALL provide a 10kΩ ±10% pull-down resistor on the PG_M2C / PRSNT_M2C signal. The module SHALL provide a 1kΩ ±10% pull-up resistor TO 3.3V.	Both	☐	☐
R9.14	The carrier SHALL pull GA0 and GA1 to defined logic levels before module power-up. GA pins SHALL NOT float.	Both	☐	☐
R10.1	Recommended EEPROM: Microchip 24AA025E48 or 24AA025E64 in the SOIC package. The A2 address pin shall be connected to Logic 0 (GND) .	Module	☐	—
R10.3	I2C addresses 0x50–0x53 reserved for FPIC EEPROM only	Module	☐	—
R11.1	GT TX AC coupling caps (100nF 0402) on module side	Module	☐	—
R11.2	GT RX AC coupling caps on carrier side	Carrier	—	☐
R11.3	IO pins ESD rated ± 2 kV HBM per JESD22-A114	Both	☐	☐
R11.4	Front-panel I/O ESD rated ± 15 kV HBM	Module	☐	—
R12.1	GT lanes 100Ω ± 10% with continuous GND plane	Both	☐	☐
R12.2	Intra-pair length mismatch ≤ 0.5mm (GT) / 2.0mm (IO)	Both	☐	☐
R12.3	GT lanes not crossing GND plane splits	Both	☐	☐
R12.4	The number of vias in GT lanes SHOULD be zero. Where vias are required, no more than one via per lane is permitted. Via stubs SHALL be backdrilled.	Both	☐	☐
R12.5	Minimum separation between adjacent differential pairs SHALL be 3× the signal trace width.	Both	☐	☐

15. FPIC Identification and Marking

All modules and carrier boards claiming compliance with the FPIC Specification **SHALL** implement the FPIC identification marking in accordance with the following requirements.

Parameter	Requirement
Marking	The appropriate FPIC designation (FPIC ST , FPIC GT4 , or FPIC GT8) SHALL be displayed on both the FPIC module and the carrier board.
Compliance	Displaying the FPIC designation is mandatory for all products claiming compliance with the FPIC Specification.
Location	The FPIC designation SHALL be placed on the Left-hand side of the FPIC connector , as shown in the mechanical drawings. The text orientation shall be parallel to the connector.
Font	Designator & Overlay: Microsoft Yahei Trademark: Montserrat Bold
Text Height	2.54mm
Colour / Finish	The FPIC designation SHALL be implemented using an Overlay .
Connector Designator	The primary FPIC connector SHALL use the reference designator P1 . Additional FPIC connectors, if present, SHALL be designated sequentially as P2 , P3 , etc.
Connector Pin Numbering	The connector pin numbers SHALL be identified on the PCB adjacent to the connector, as illustrated in the image below. Pin numbering SHALL clearly indicate the first and last pin locations and maintain the numbering sequence defined by the FPIC connector specification to ensure correct module orientation and assembly.
Visibility	The FPIC designation SHALL remain unobstructed by components, heatsinks, labels, or other mechanical features to ensure clear identification.

FPIC Connector Identification	<p>For carrier boards implementing a single FPIC connector, the PCB overlay SHALL identify the connector as “FPIC ST” or “FPIC GT4 / FPIC GT8”, as applicable. For carrier boards implementing multiple FPIC connectors of the same or different standards, each connector SHALL be assigned a unique identifier A, B, C, or D. The PCB overlay SHALL display the identification in the format “FPIC <FPIC Standard> <Connector Assignment>”. For example, multiple FPIC ST connectors shall be marked “FPIC ST A”, “FPIC ST B”, “FPIC ST C”, and so on; similarly, multiple FPIC GT connectors shall be marked “FPIC GT8 A”, “FPIC GT8 B”, “FPIC GT4 C”, and so on. The identification SHALL be placed adjacent to the corresponding connector, as shown in Figure 18.</p>
FPIC Logo	<p>The FPIC logo (PNG format) SHALL be placed to the right of the FPIC connector on the PCB overlay, as shown in the reference image below.</p> 

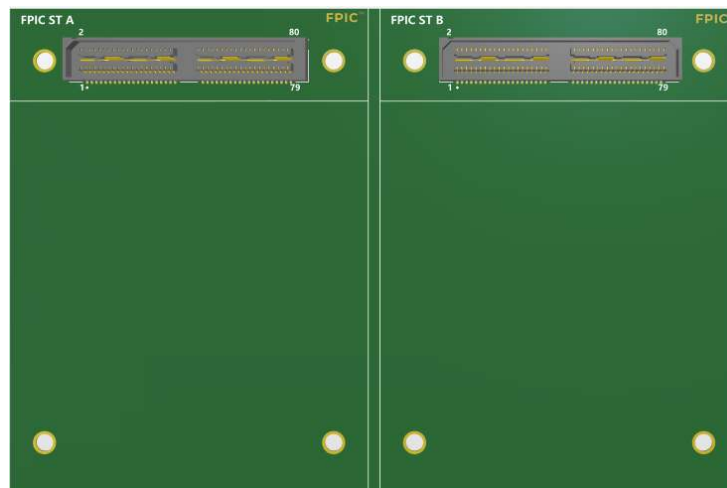


Figure 19: FPIC Carrier

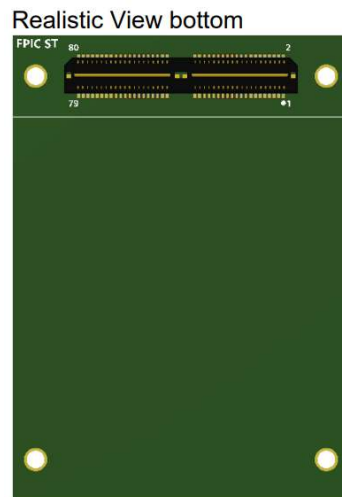


Figure 20: FPIC Module

Note: The placement, orientation, and dimensions of the FPIC designation shall conform to the mechanical drawings provided in this specification to ensure a consistent appearance across all FPIC compliant modules and carrier boards.

16. Acknowledgements

The FPIC standard was developed by **Numato Systems Pvt Ltd**. The connector system is based on the Samtec **QTE/QSE (FPIC ST)** and **QTH/QSH (FPIC GT)** high-speed board-to-board connector families.