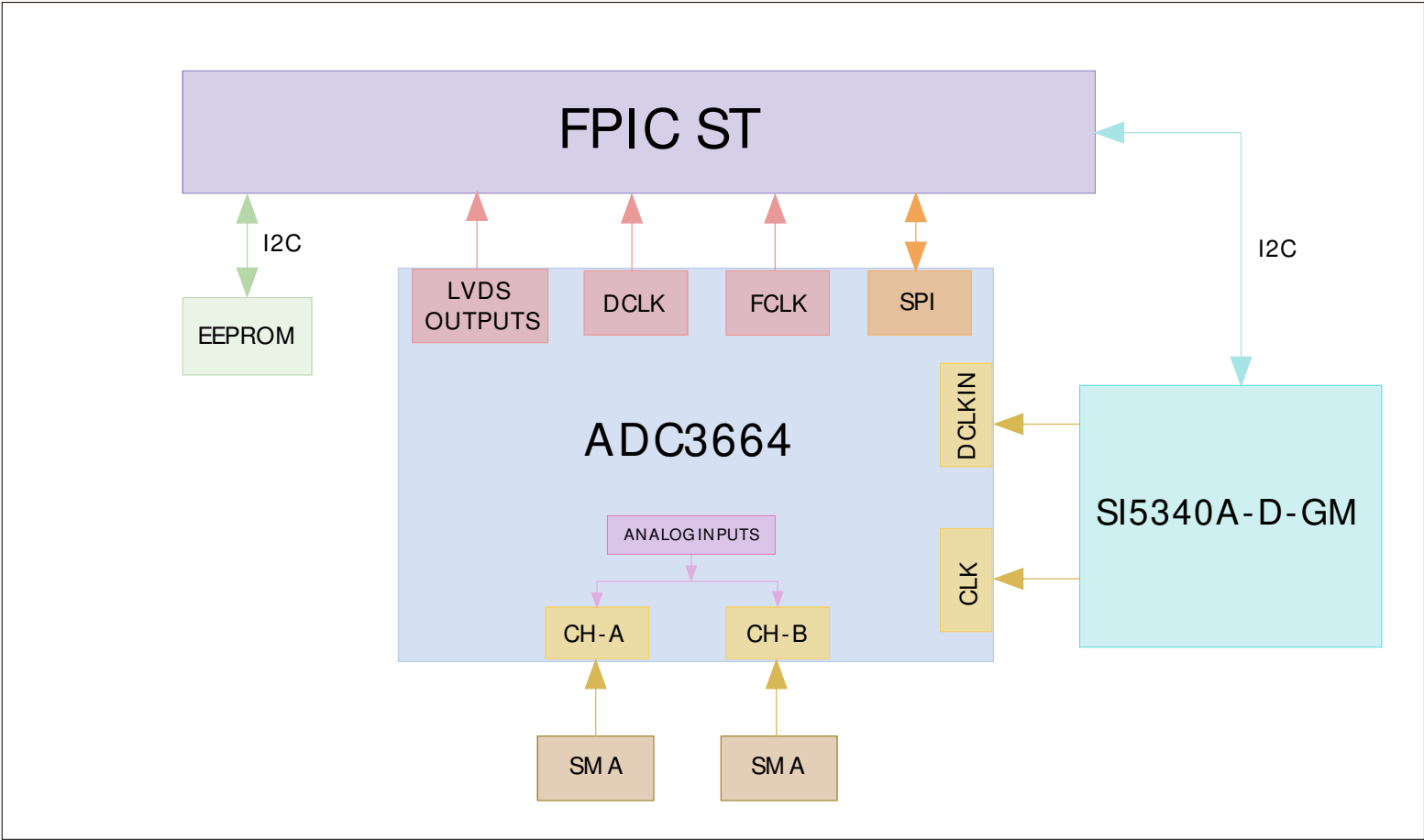
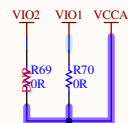


Sheet No	Contents	Sheet Name
1	Block diagram	BLOCK DIAGRAM
2	FPIC HEADER, EEPROM, POW STATUS LED	FPIC ST
3	ADC3664	ADC
4	CLOCK GENERATOR	ADC CLK

BLOCK DIAGRAM









ADC

The image displays a detailed schematic of an ADC system, specifically the ADC3644HSBT, and its associated interface components. The main schematic shows the ADC chip connected to various power supplies (AVDD, IOVDD, IOGND) and ground. It includes input buffers (AINP, AINM, etc.), clock inputs (CLKP, CLKM), and output pins (DA0P, DA0N, etc.). The system is powered by a 1.6V reference voltage (VREF) and a 1.6V supply (VDD1V3). The ADC is connected to an FPGA via an SDI to ADC SDIO interface, which includes a buffer (U4) and resistors (R62, R63, R64). The ADC also has a reset switch (SW1) and a pull-down resistor (R3) connected to its RESET pin. The power supply decoupling is shown with various capacitors (C2, C3, C4, C5, C6, C7, C8, C9, C10, C14, C37, C38, C39) and inductors (FB1, FB2) connected to the power and ground pins. The signal conditioning section shows the connection of the input signal (SDI) to the ADC input (SDIO) through a buffer and resistors.

FPGA SDI to ADC SDIO interface

VREF (1.6V)

RESET SWITCH

Power supply decoupling

Signal conditioning

ANALOG INPUTS

CHA_P

CH-A

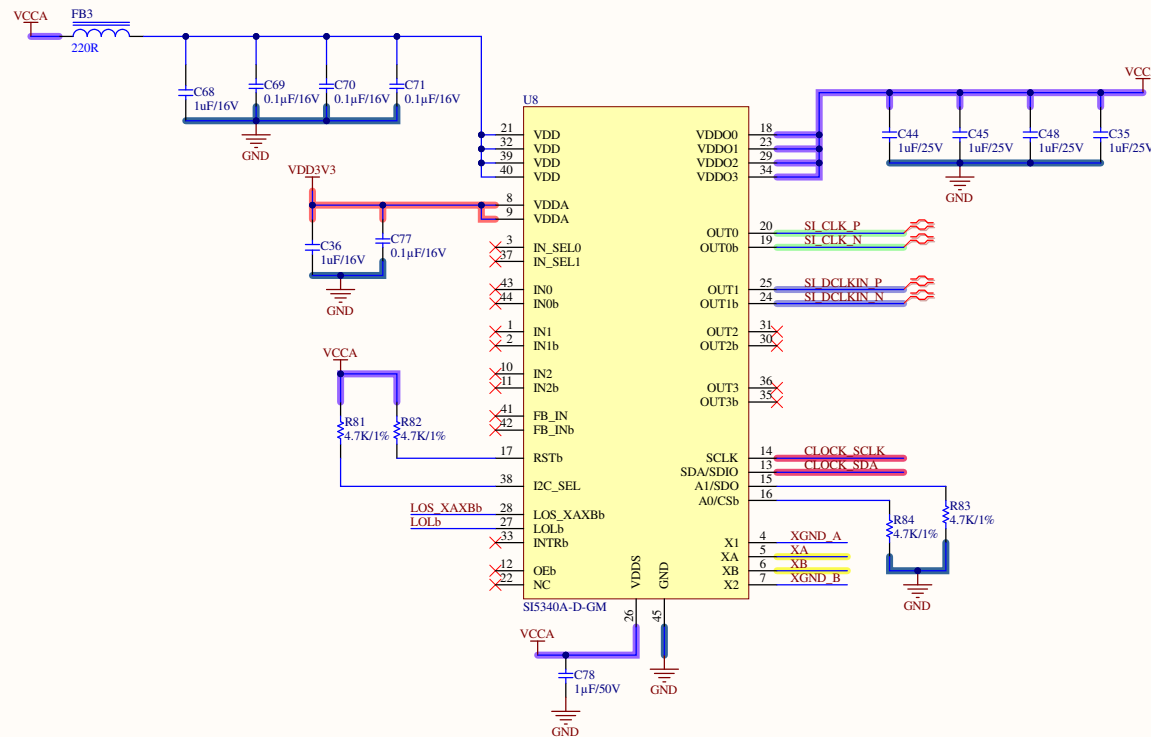
CHA_N

CHB_N

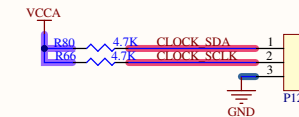
CH-B

CHB_P

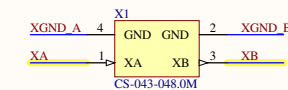
CLOCK GENERATOR



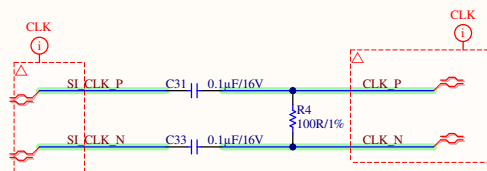
12C HDR



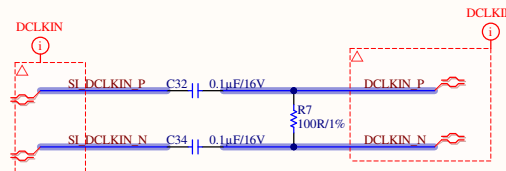
CRYSTAL 48MHz



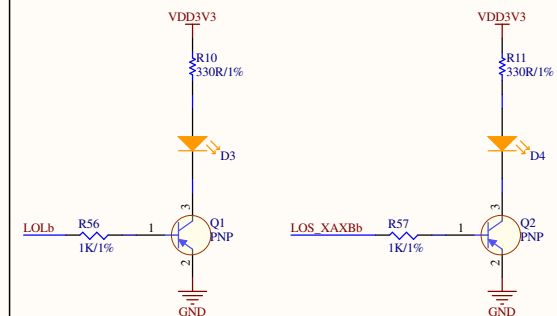
SAMPLING CLK



DCLKIN



Fault Indication



Title: ADC INPUTS

Revision: A1

Size: A3 Project: FPICST004.PrjPcb

Date: 15.02.2026 Time:09:05:07

File: ADC CLK.SchDoc

Sheet 4 of 4

Numato Lab