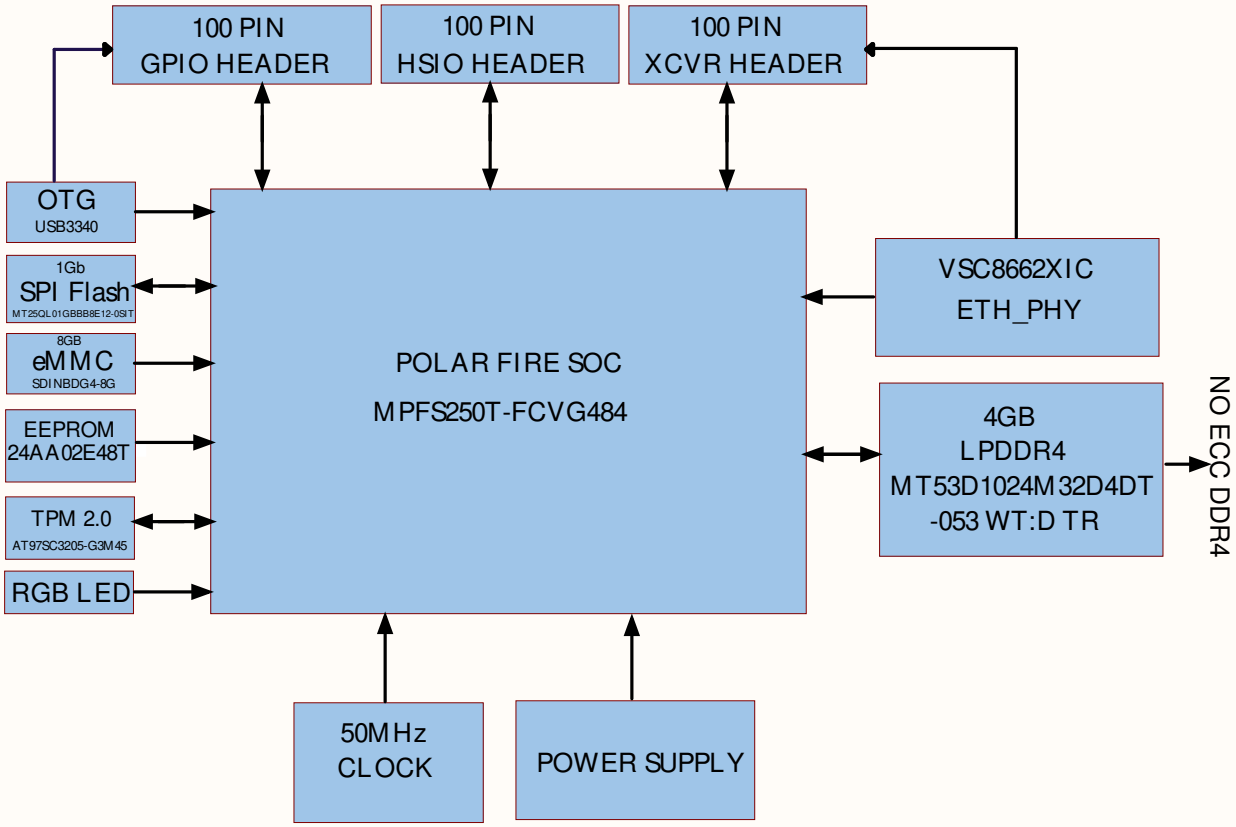
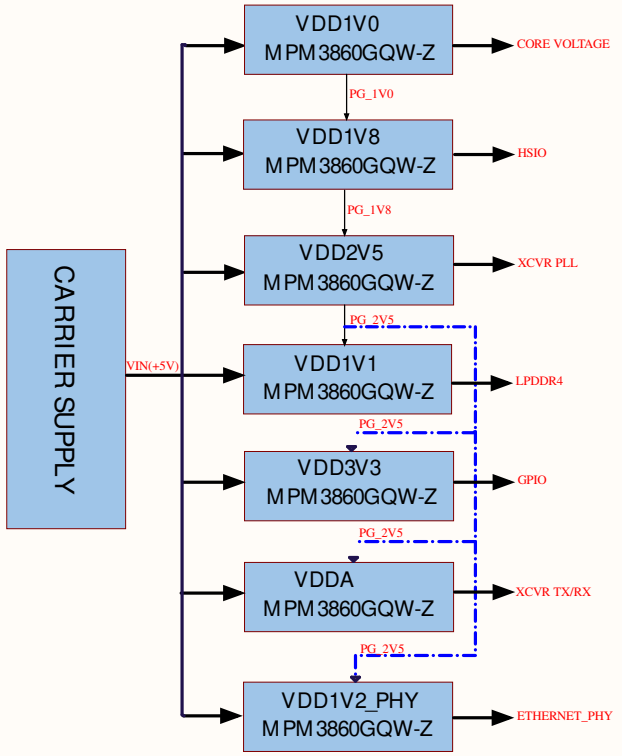
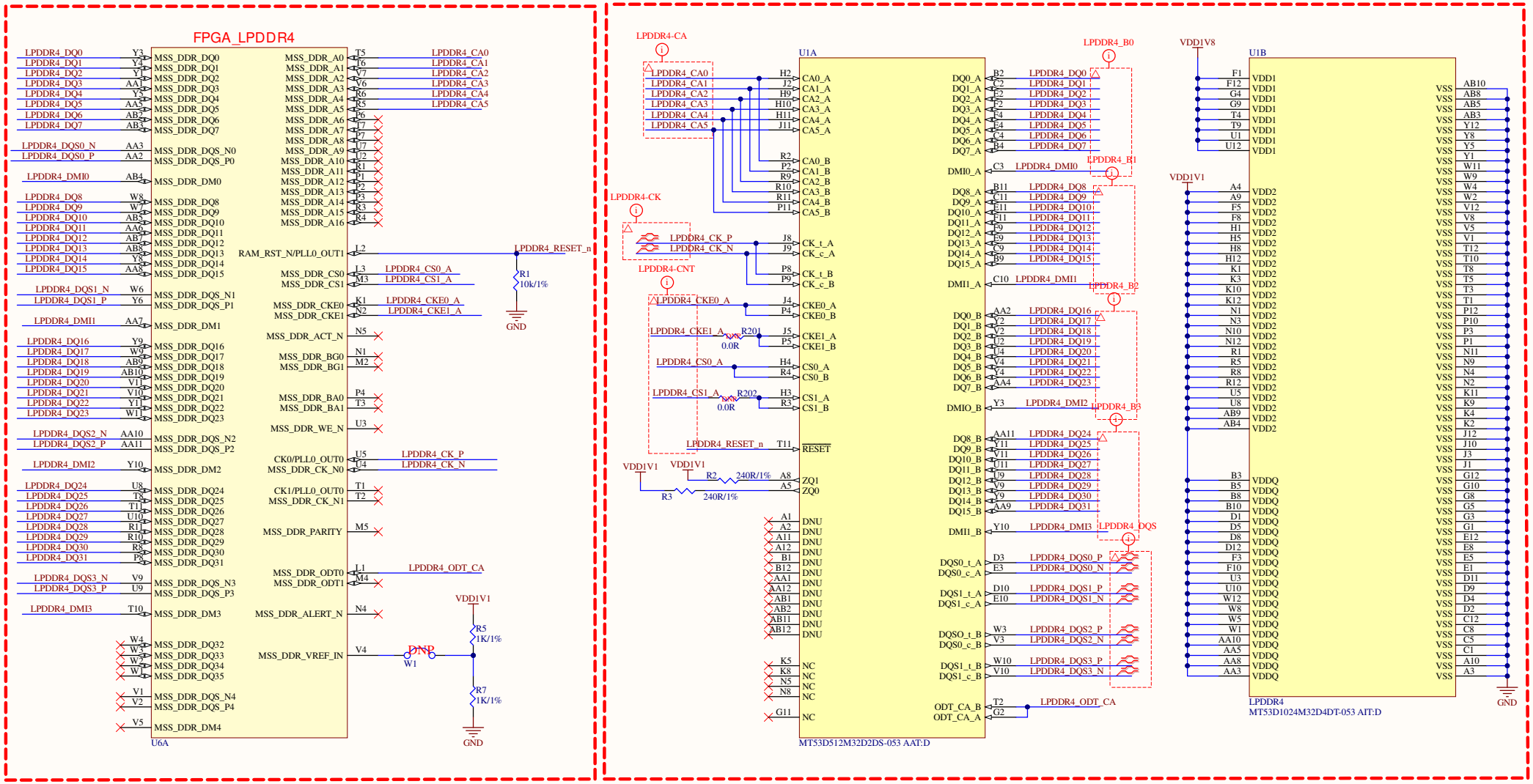
BLOCK DIAGRAM





Title: Block diagram		Revision: V1.0	Numato Lab
Size: A2	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:32	Sheet 1 of 13	
File: Block diagram.SchDoc			



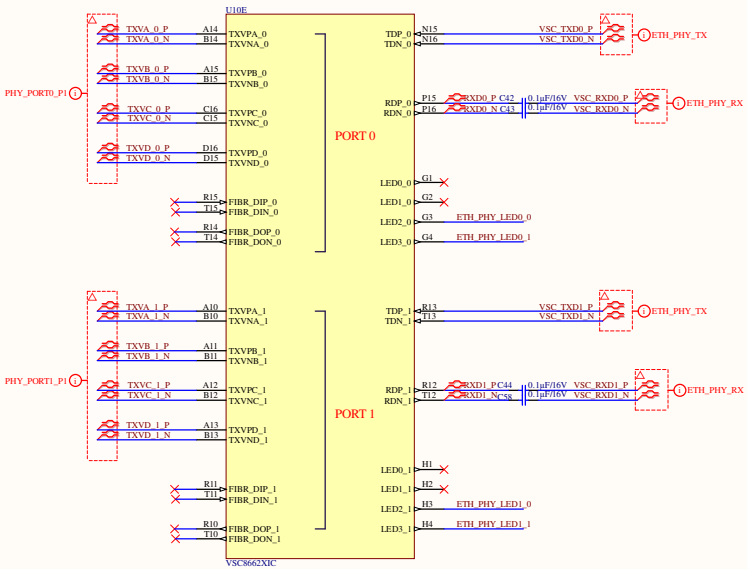
FPGA BANK 6

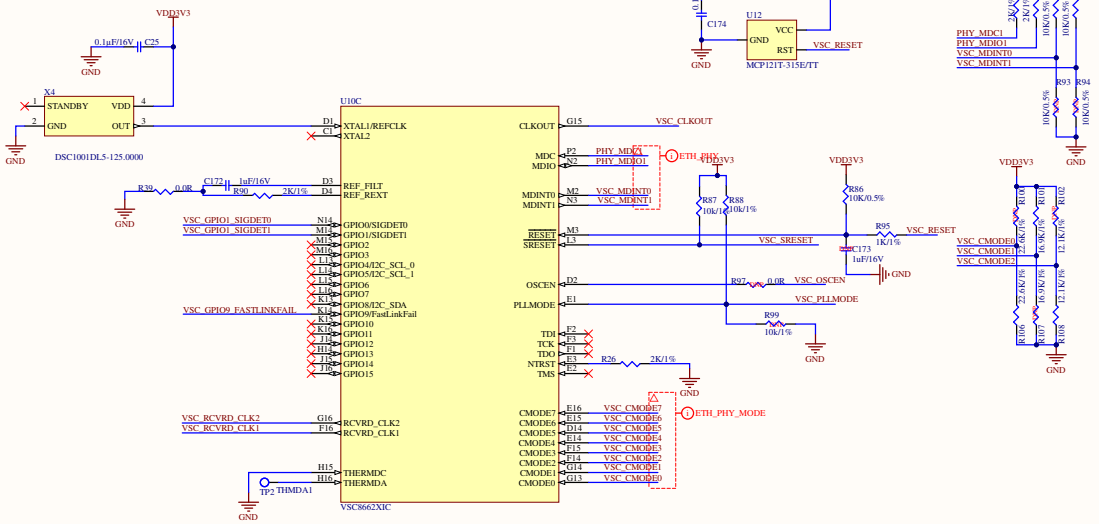
LPDDR4

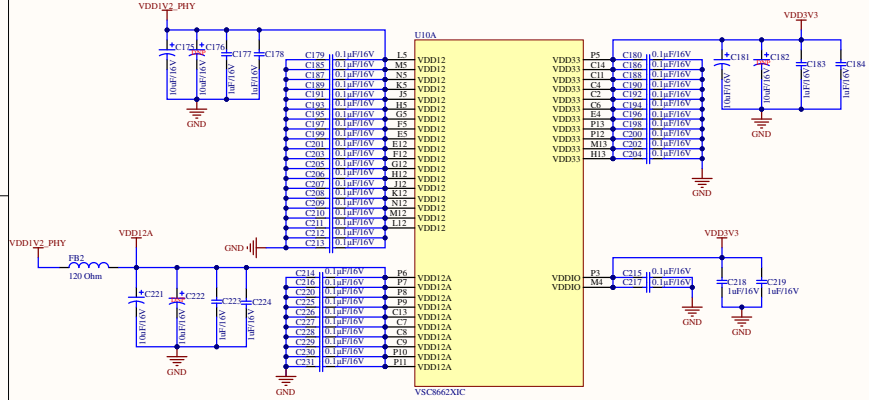
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Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:33	Sheet 2 of 13	
File: LPDDR4.SchDoc			

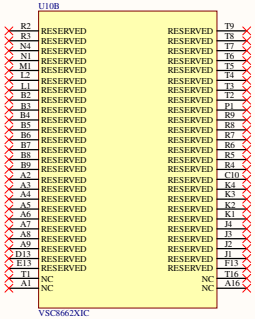
Numato Lab

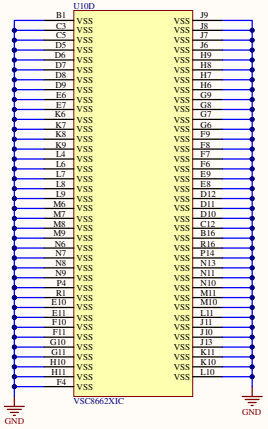
ETHERNET_PHY



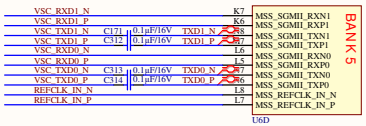


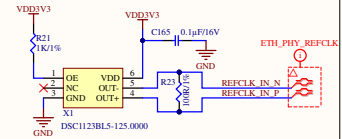






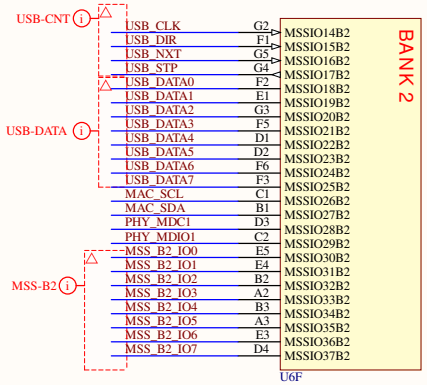
SGMII_BANK



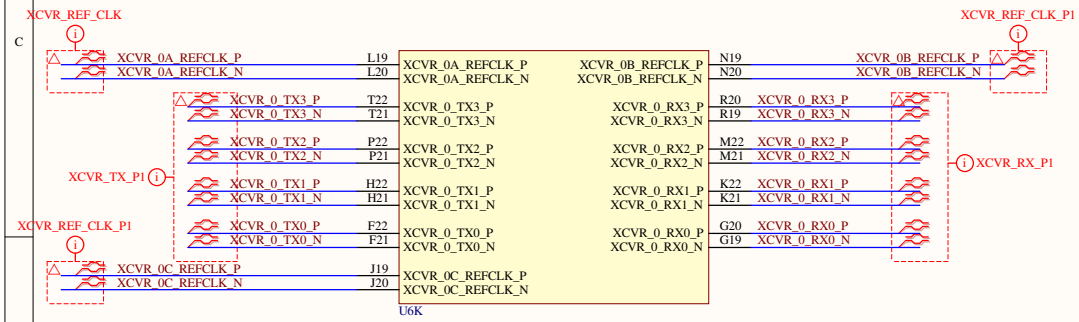


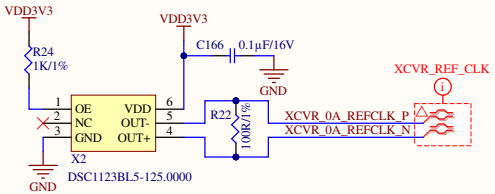
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Size:	A2	Project:	NL-FMPS-B-001.PrjPcb
Date:	02-07-2024	Time:	15:49:34
Sheet	3 of 13		
File:	Ethernet_PHY.SchDoc		

NumatoLab



XCVR interface

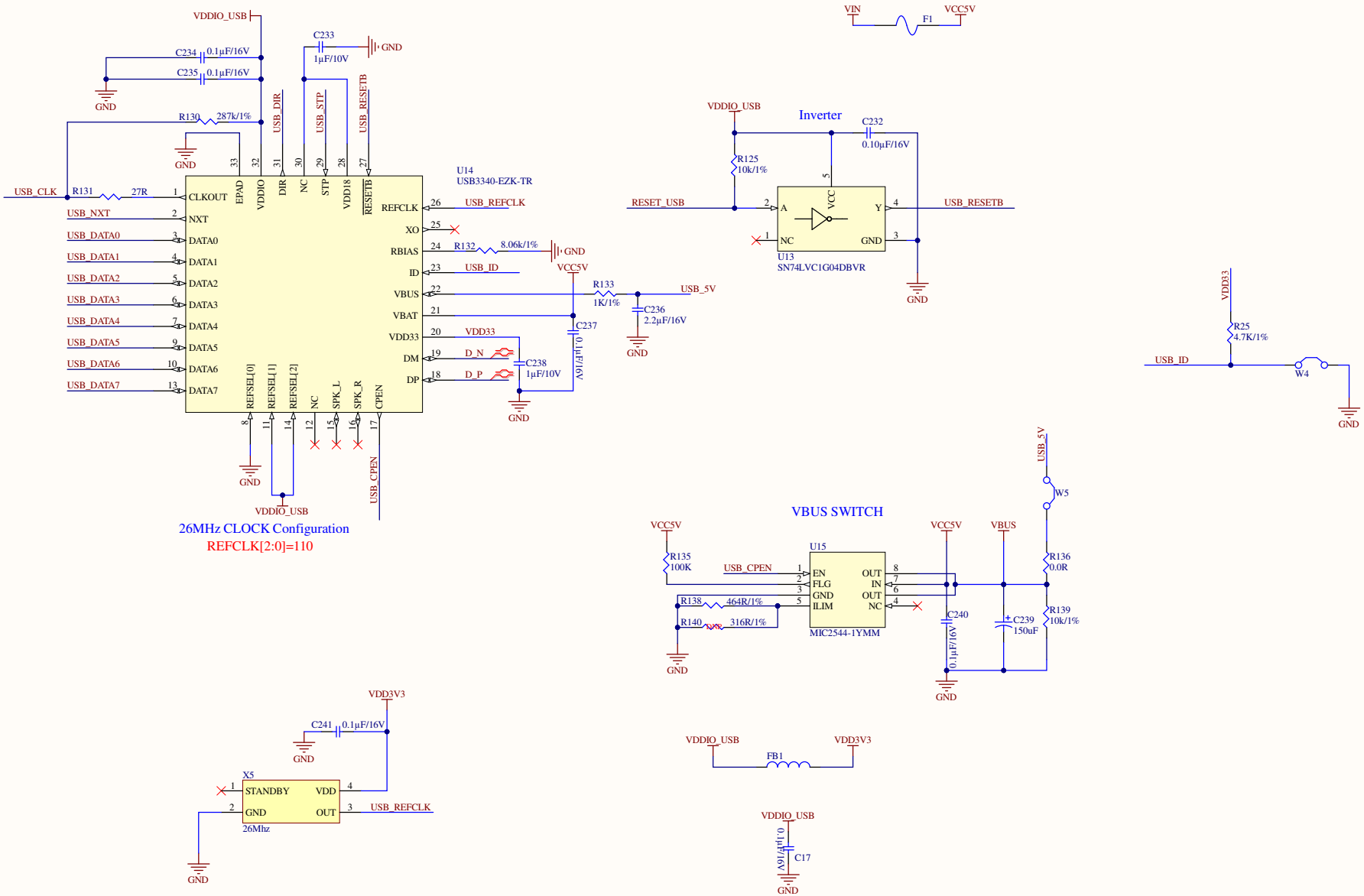




CLOCK BUFFER 125MHz

Title: MSSIO		Revision: V1.0	Numato Lab
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:35	Sheet 4 of 13	
File: MSSIO-XCVR.SchDoc			

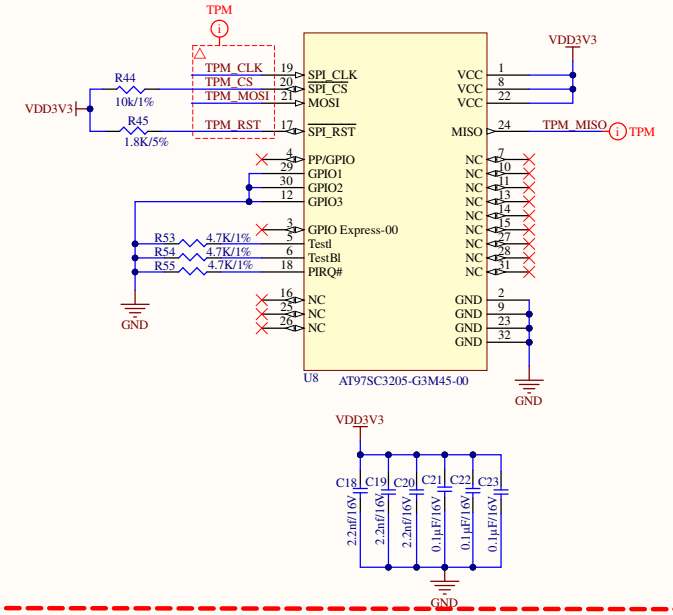
USB_OTG



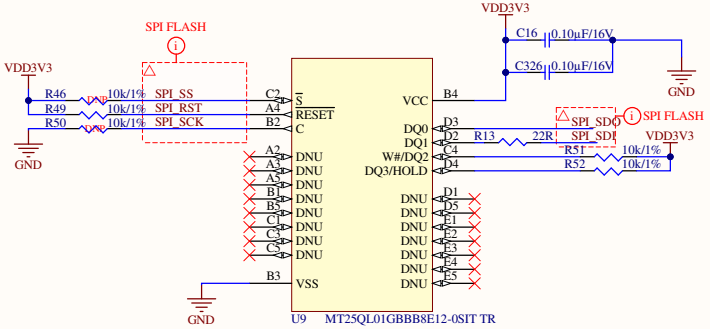
Title: USB-OTG		Revision: V1.0	
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:36	Sheet 5 of 13	
File: OTG.SchDoc			

Numato Lab

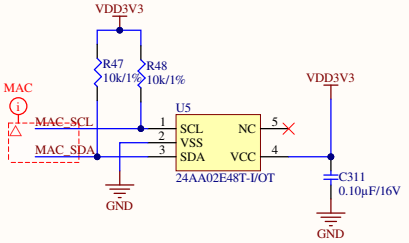
TPM



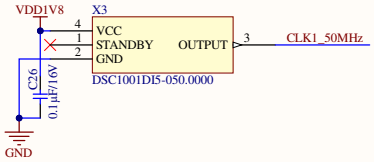
SPI FLASH



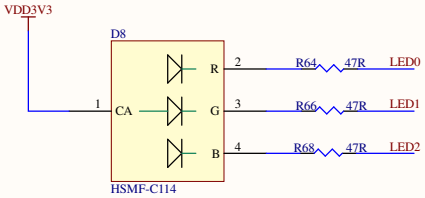
EEPROM

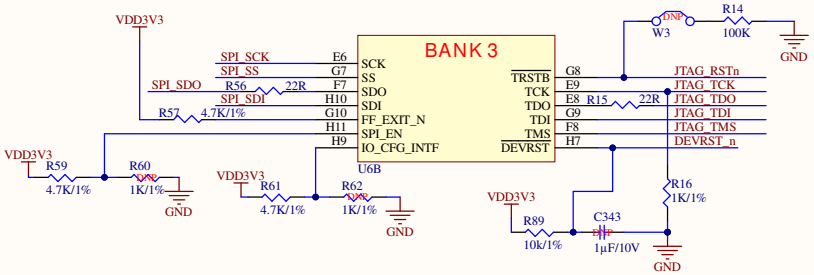


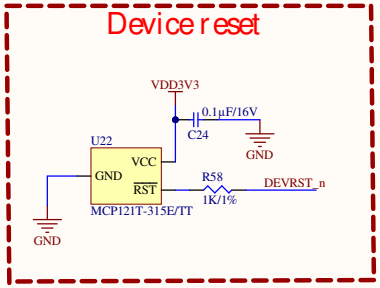
CLOCK 50MHz



RGB

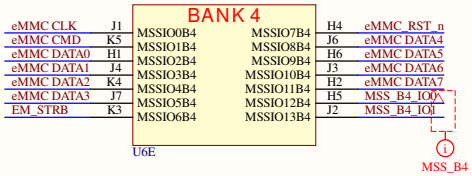


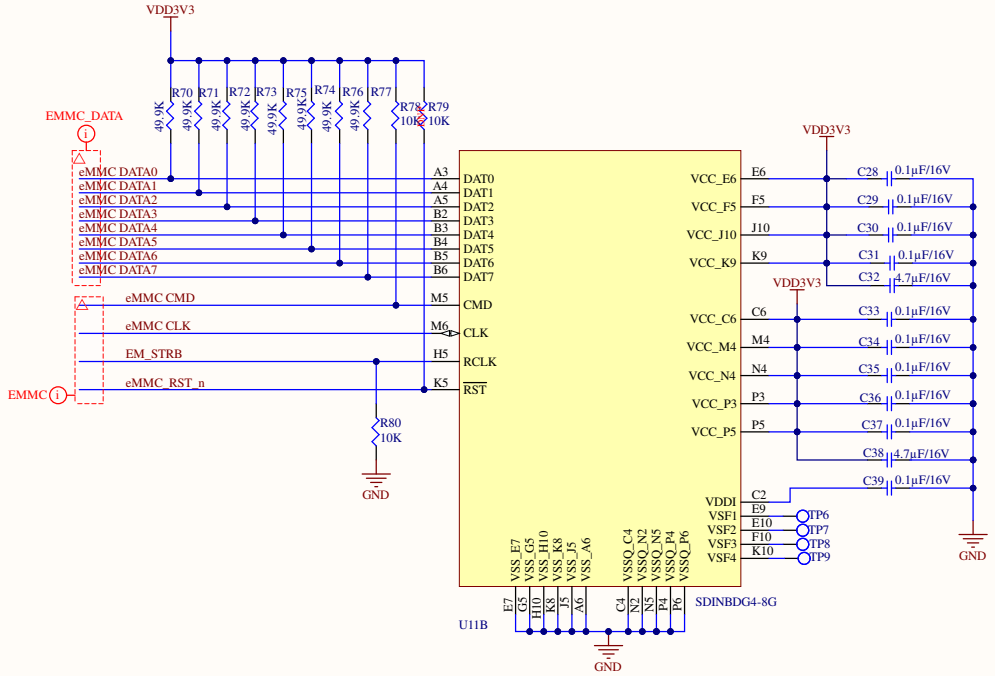


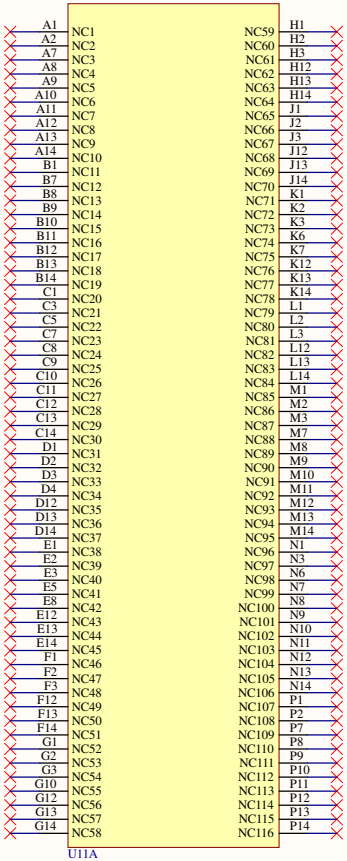


Title: Peripherals		Revision: V1.0	Numato Lab
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:36	Sheet 6 of 13	
File: Peripheral.SchDoc			

eMMC

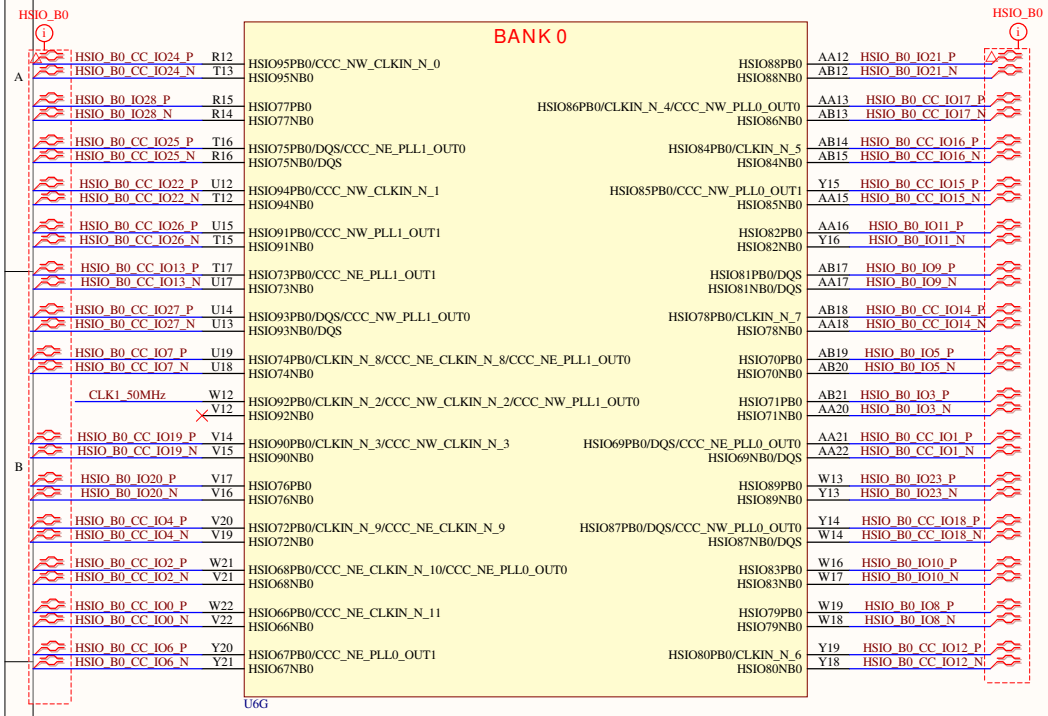


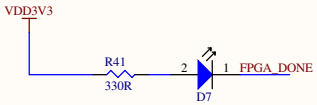




Title: EMMC		Revision: V1.0	Numato Lab
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:37	Sheet 7 of 13	
File: eMMC.SchDoc			

HSIO-FPGA

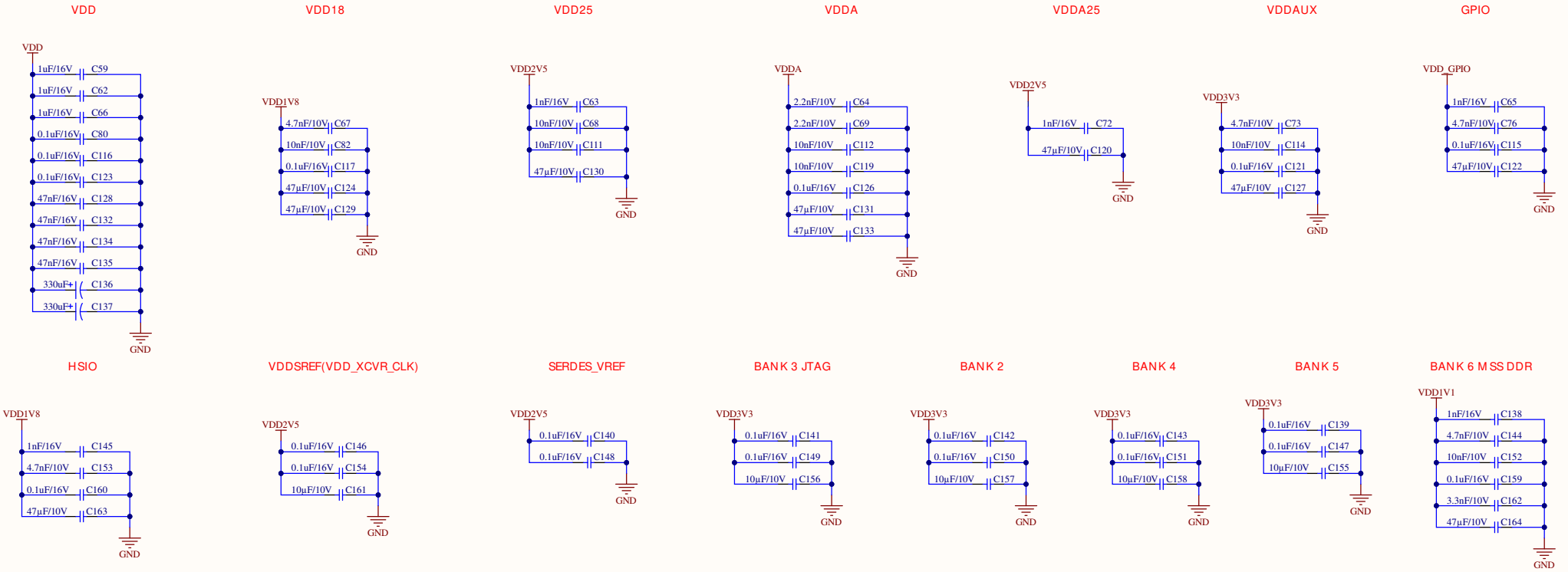




GPIO-FPGA

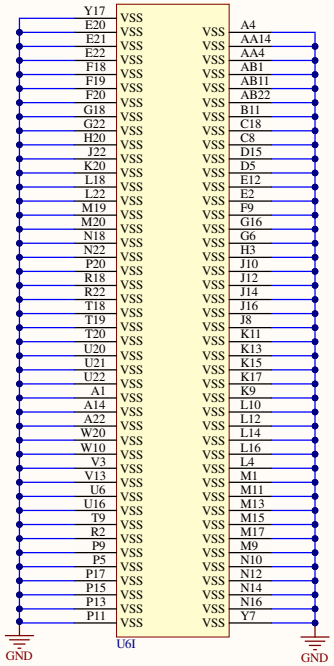


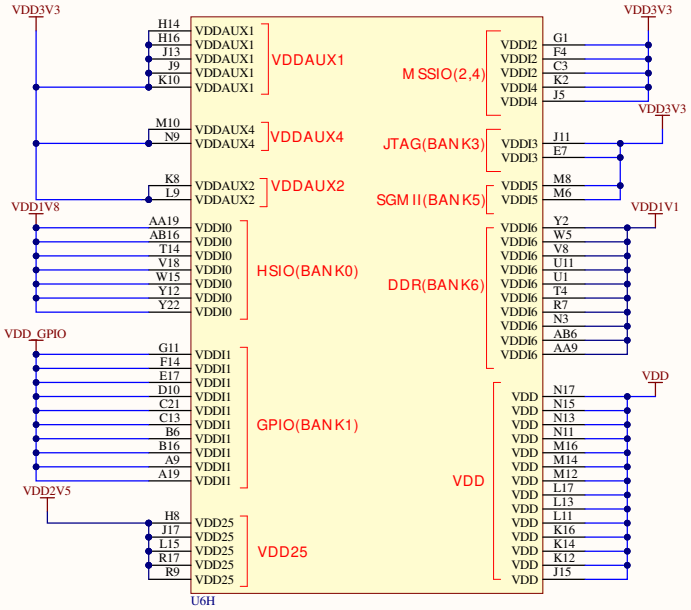
Title: GPIO/HSIO		Revision: V1.0	Numato Lab
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:38	Sheet 8 of 13	
File: HSIO-GPIO.SchDoc			

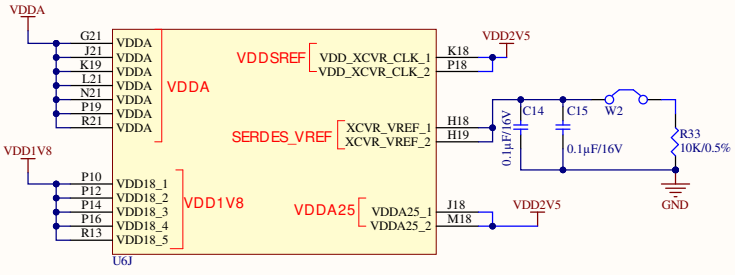


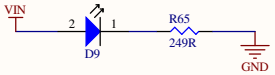
Title: Decoupling capacitor		Revision: V1.0	Numato Lab
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:39	Sheet 9 of 13	
File: Decoupling capacitor.SchDoc			

FPGA POWER







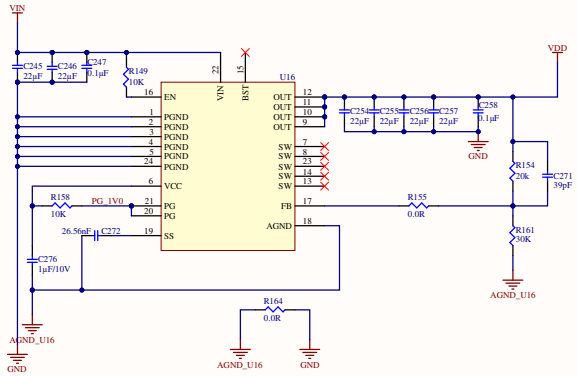


Title: POWER		Revision: V1.0	
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:40	Sheet 10 of 13	
File: FPGA power.SchDoc			

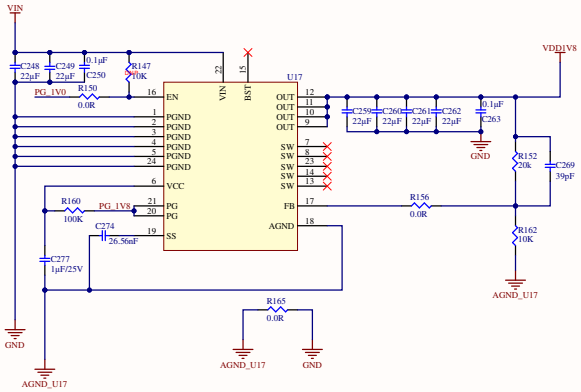
Numato Lab

PWR_Supply

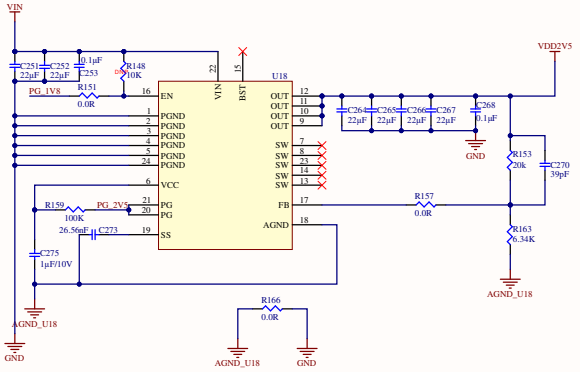
POWER VDD1V0



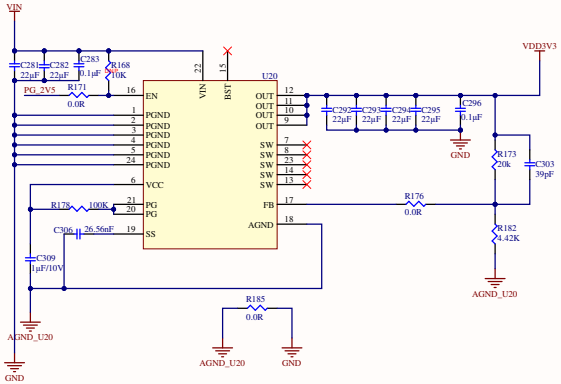
POWER VDD1V8



POWER VDD2V5

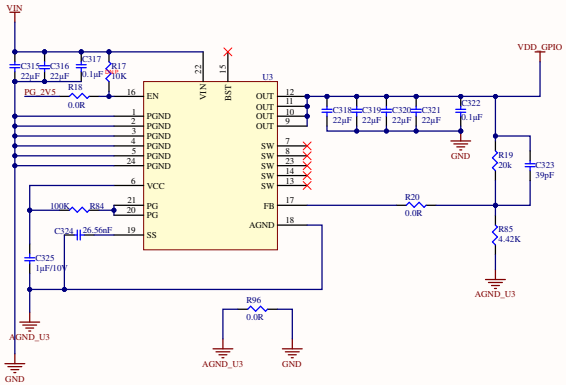


POWER VDD3V3

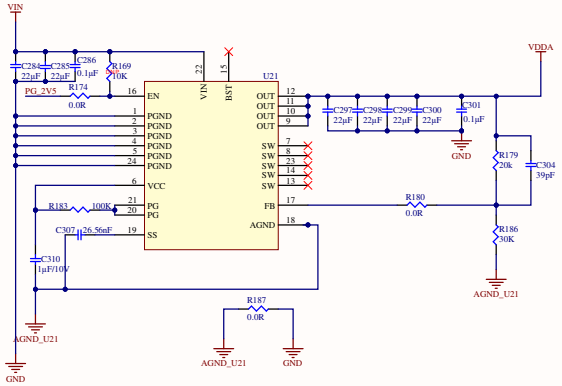


PG_2V5 R198 0.0R PG_ALL

POWER GPIO



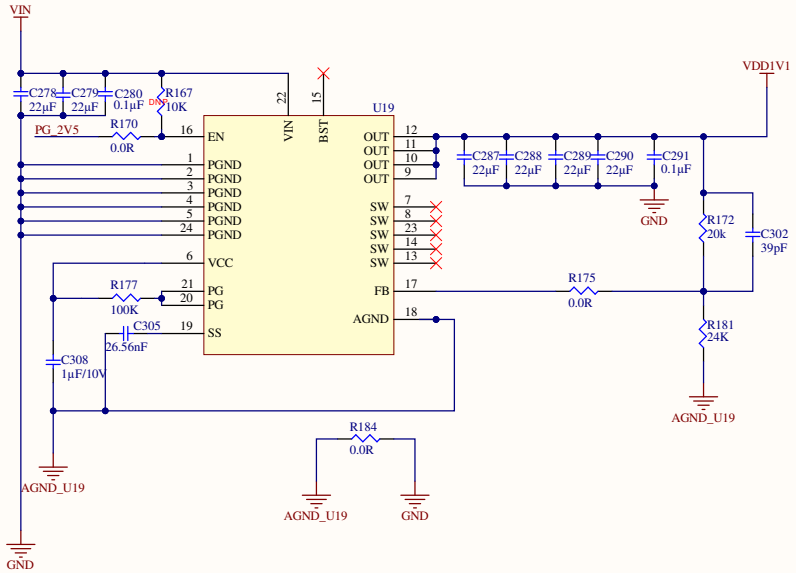
POWER VDDA(1.05v)



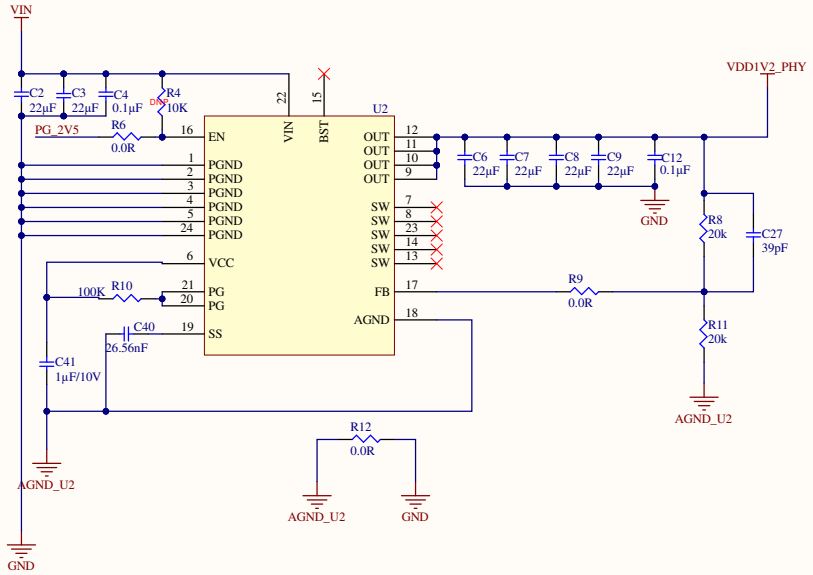
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Size:	A2	Project:	NL-FMPS-B-001.PrjPcb
Date:	02-07-2024	Time:	15:49:40
Sheet	11 of 13	File:	Core supply.SchDoc

Numato Lab

POWER LPDDR4 VDD1V1



Ethernet_PHY power



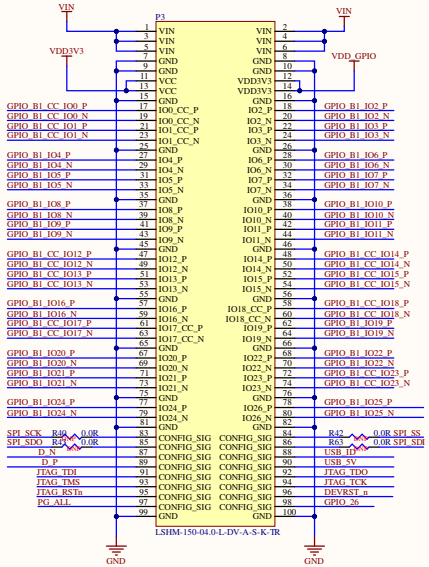
P4 FD 1mm fudiual

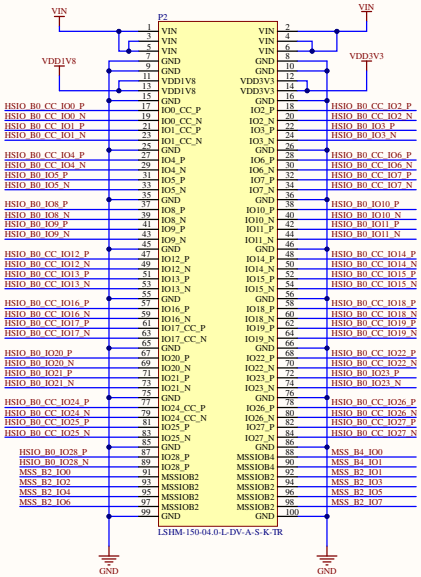
P5 FD 1mm fudiual

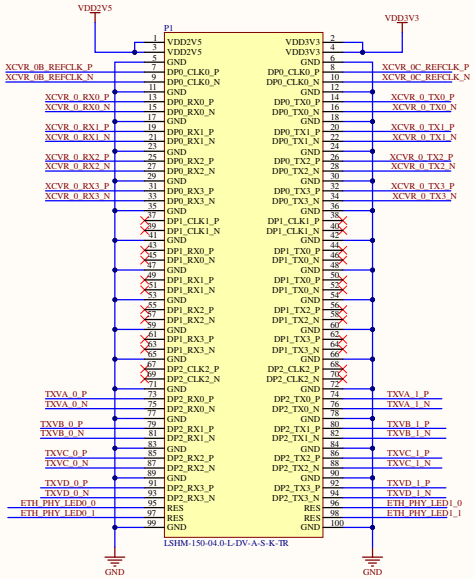
P6 FD 1mm fudiual

Title: Periperal supply		Revision: V1.0	Numato Lab
Size: A3	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:41	Sheet 12 of 13	
File: Periperals supply.SchDoc			

MODULE GPIO CONNECTOR







Title: GPIO		Revision: V1.0	Numato Lab
Size: A2	Project: NL-FMPS-B-001.PrjPcb		
Date: 02-07-2024	Time: 15:49:42	Sheet 13of 13	
File: Connector.SchDoc			