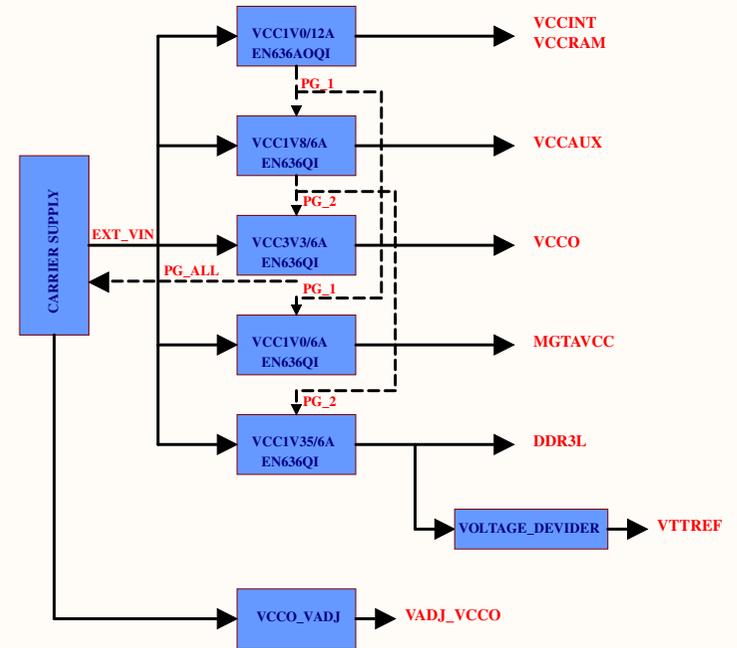
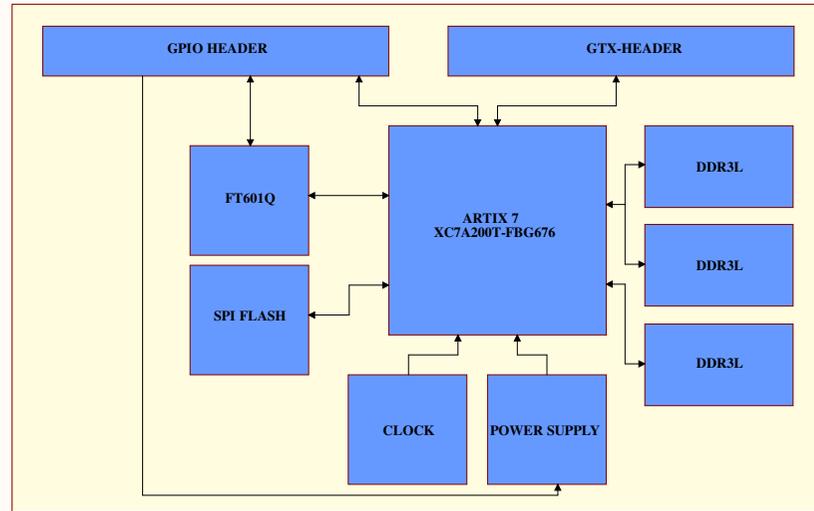
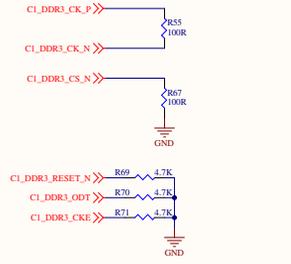
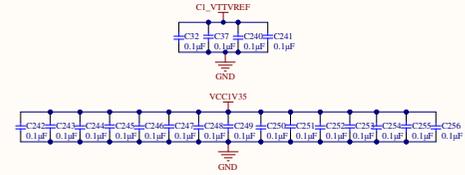
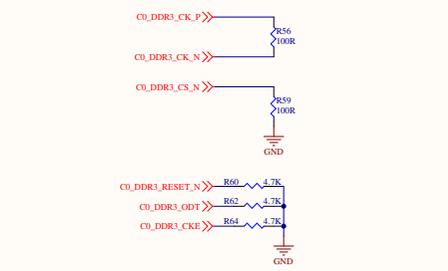
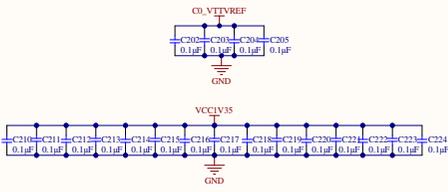
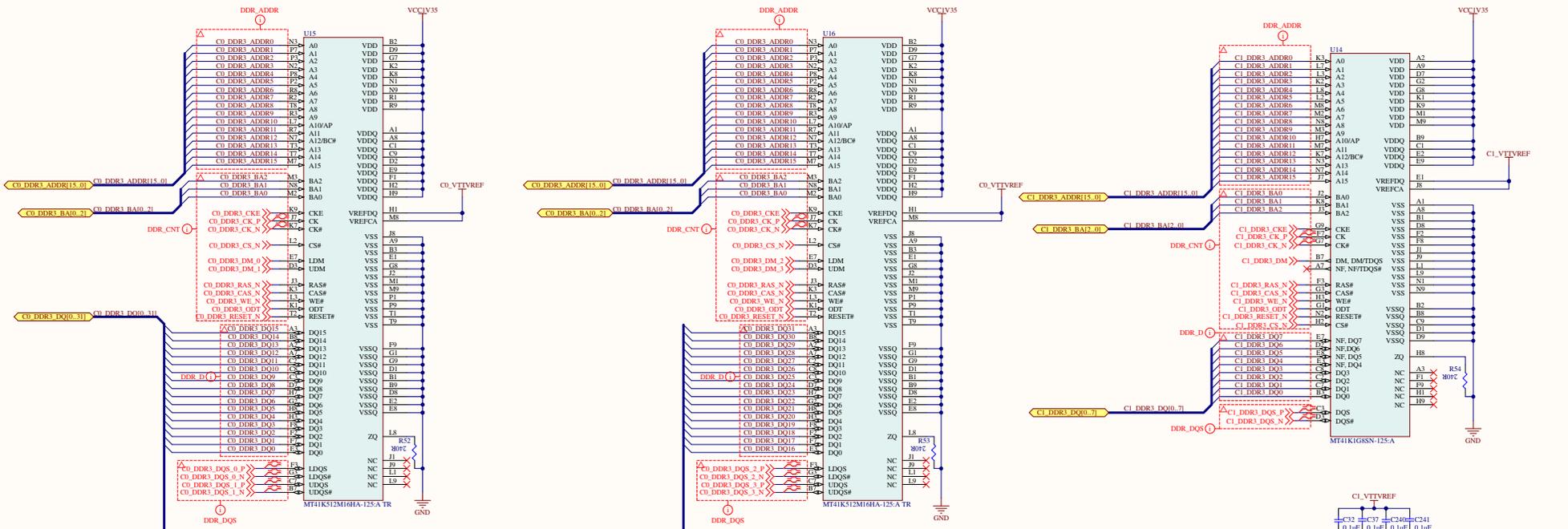


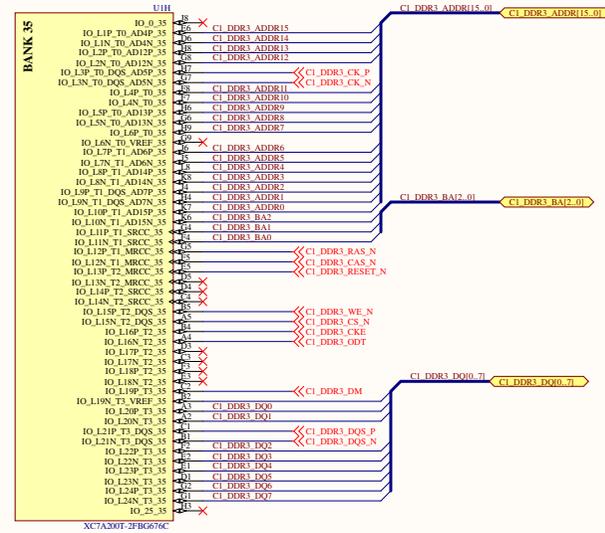
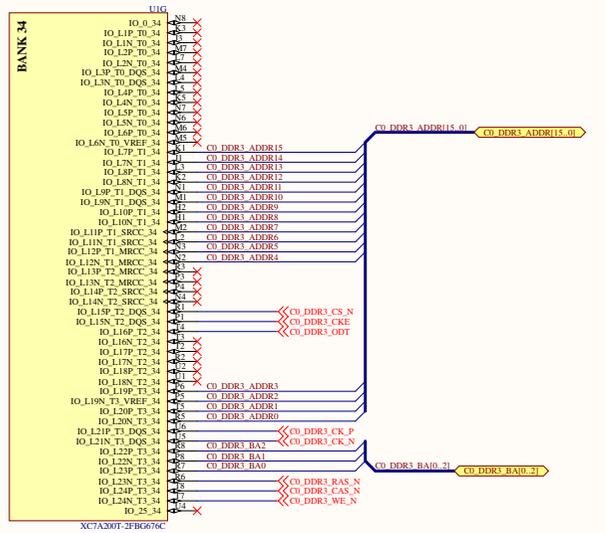
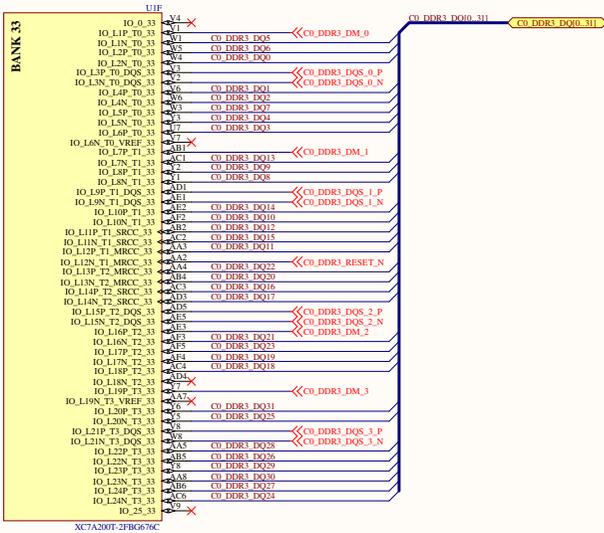
## BLOCK DIAGRAM



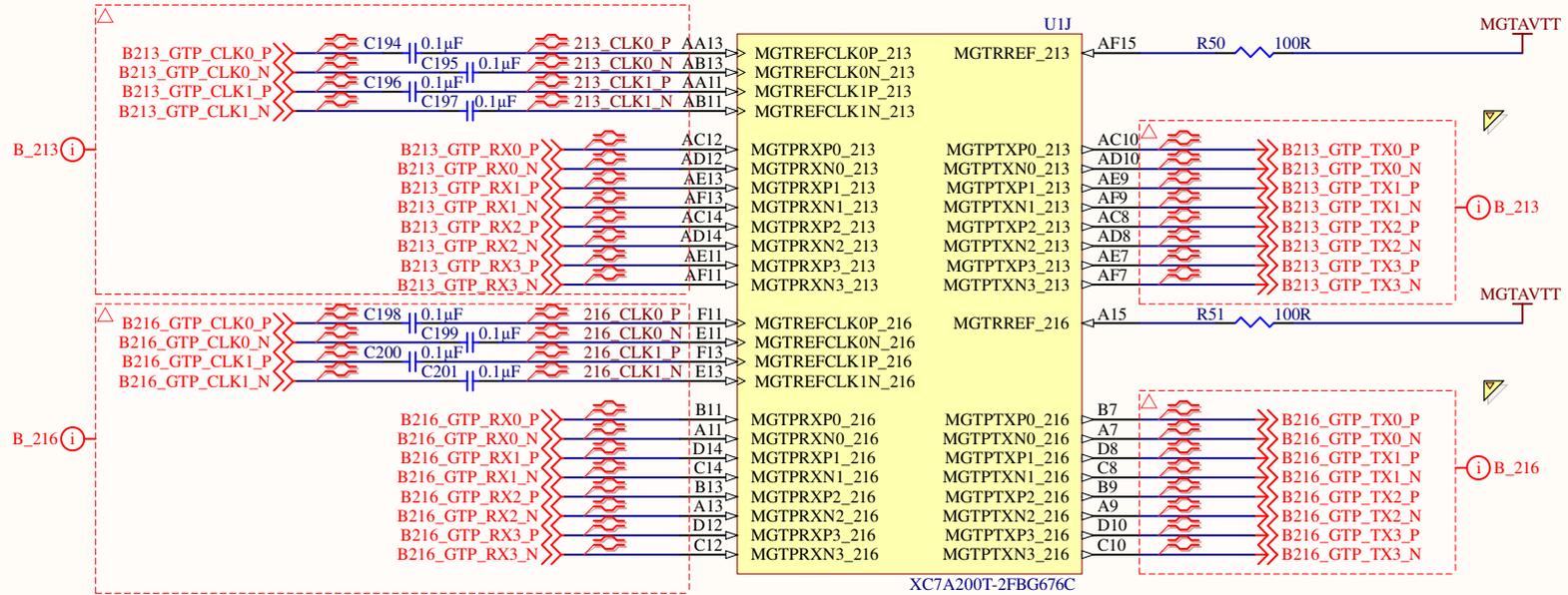
# DDR3L SECTION



FPGA DDR3



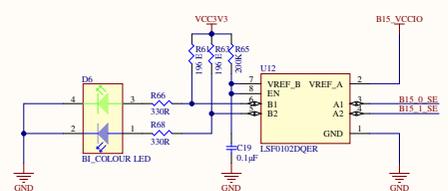
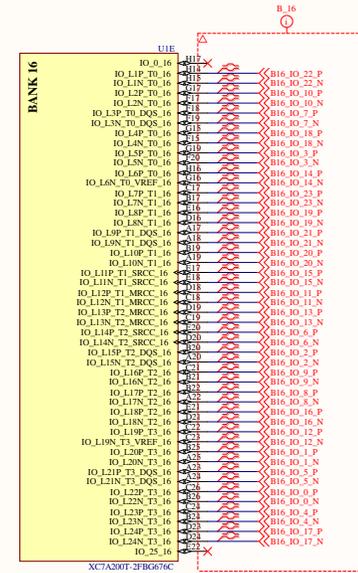
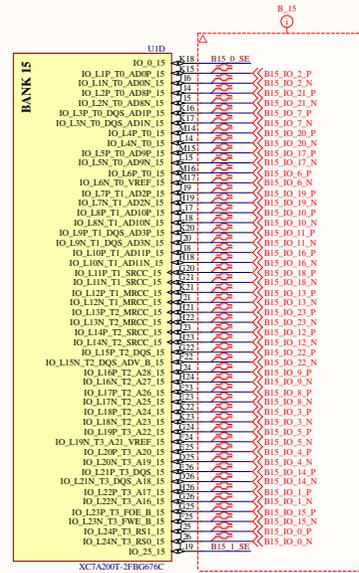
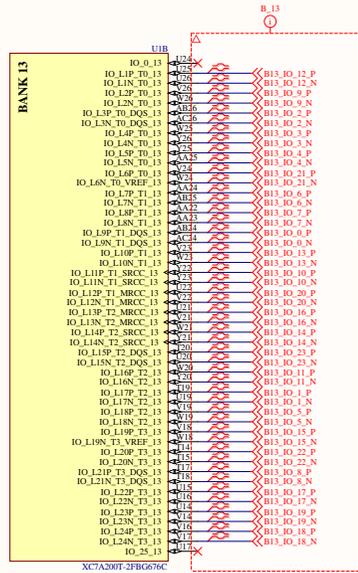
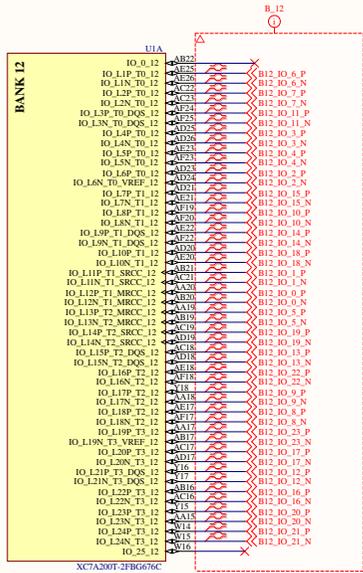
# FPGA GTP



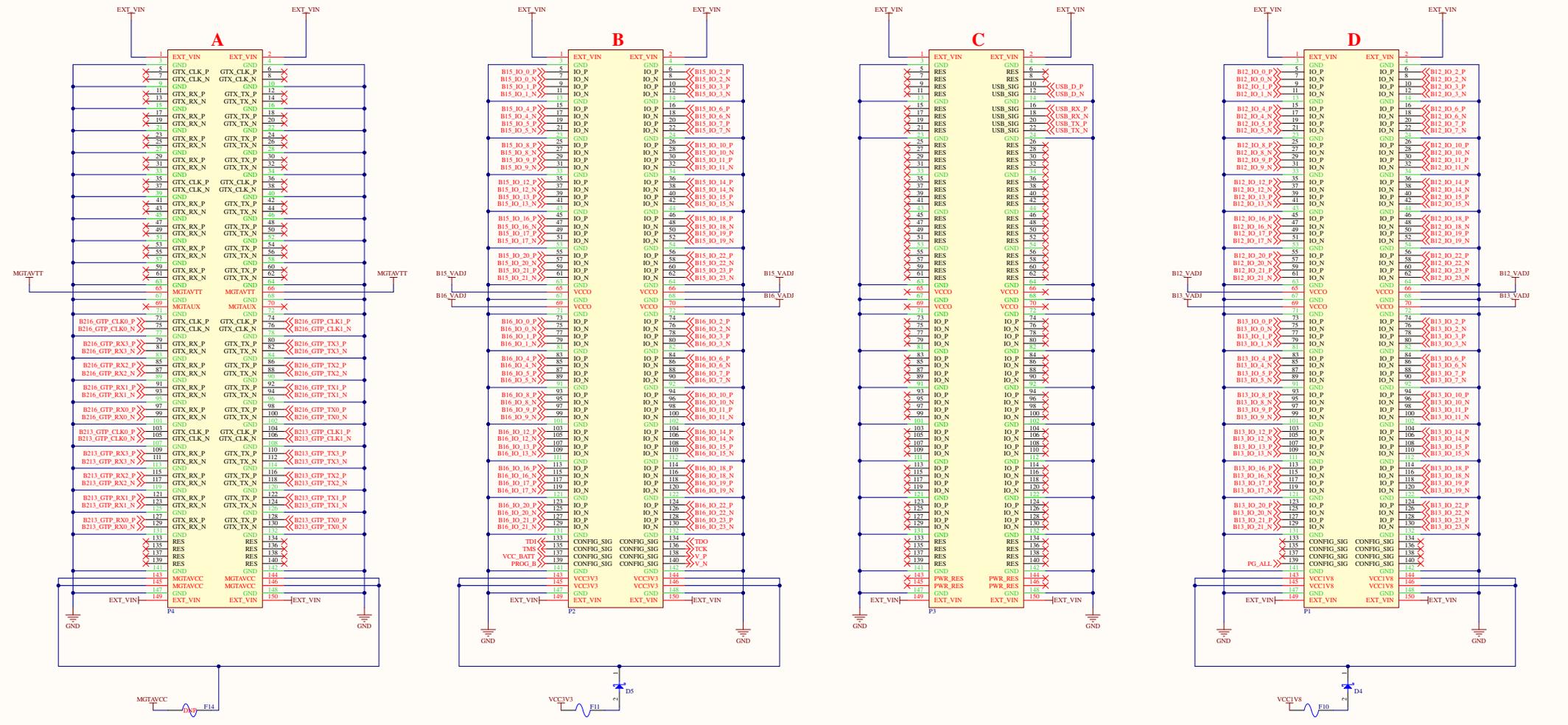
XC7A200T-2FBG676C

Title: <b>FPGA GTP</b>		Revision: V 1.1	 <b>Numato System Pvt Ltd</b>
Size: A4	Project: Nile_Board.PrfPcb		
Date: 20-01-2021	Time: 14:38:52	Sheet 4 of 10	
File: FPGA_GTP.SchDoc			

# FPGA GPIO

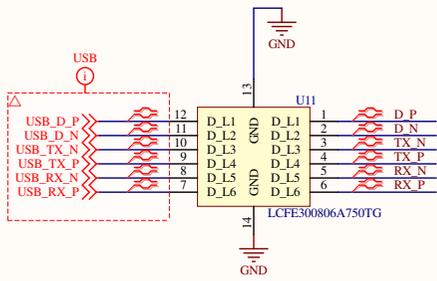


# GPIO CONNECTOR

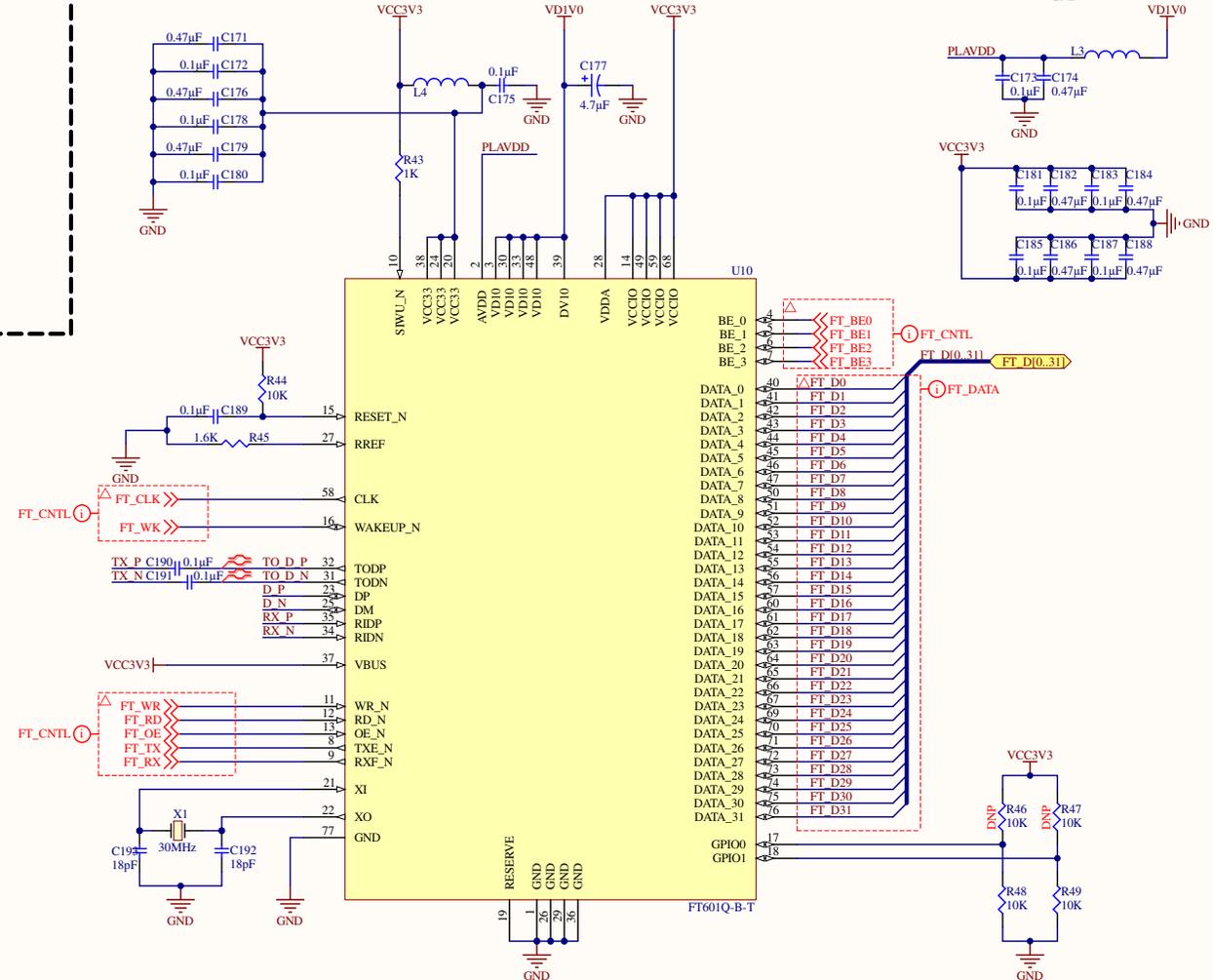




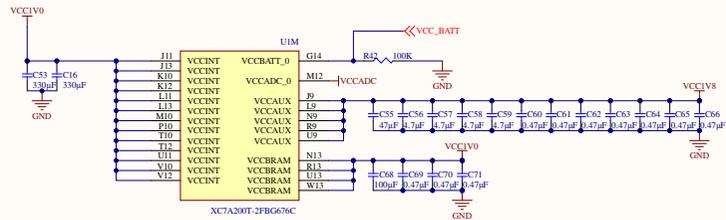
### USB ESD



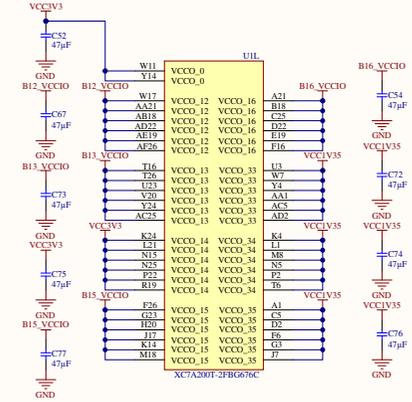
### USB FT601



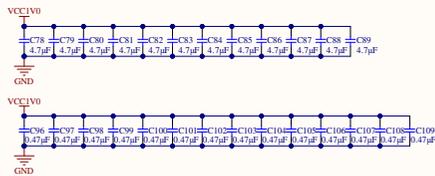
### FPGA VCCINT, VCCBRAM, VCCAUX POWER



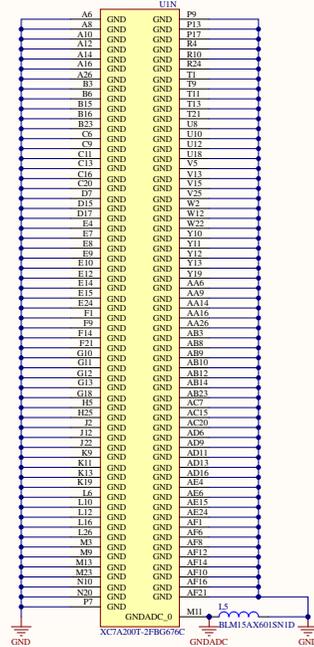
### FPGA VCCO POWER



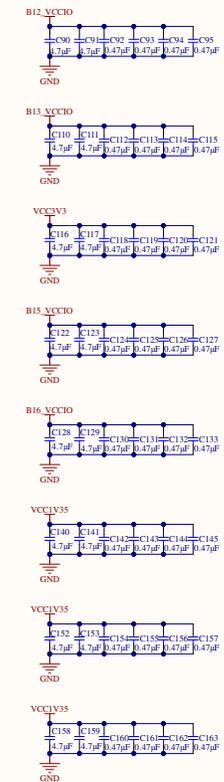
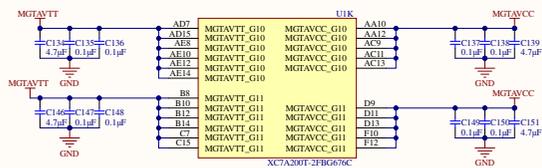
### VCCINT DECOUPLING CAP



### FPGA GND

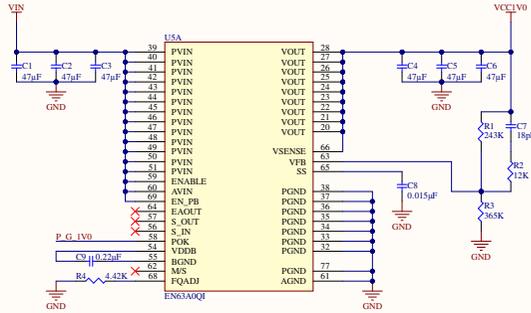


### FPGA GTP POWER

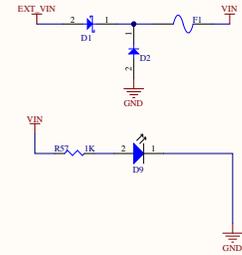


### POWER VCC1V0

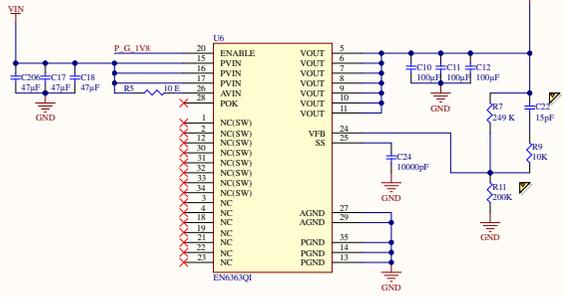
Pin	Signal	Value
1	NC	NC(SW)
2	NC	NC(SW)
3	NC	NC(SW)
4	NC	NC(SW)
5	NC	NC(SW)
6	NC	NC
7	NC	NC
8	NC	NC
9	NC	NC
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	NC
15	NC	NC
16	NC	NC



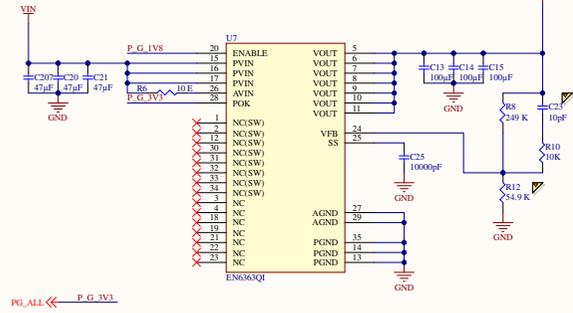
### EXT POWER



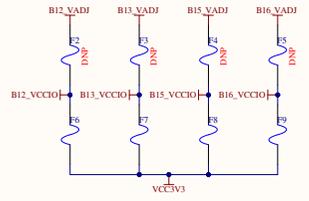
### POWER VCC1V35



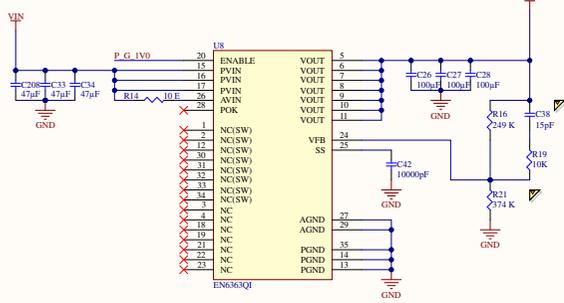
### POWER VCC3V3



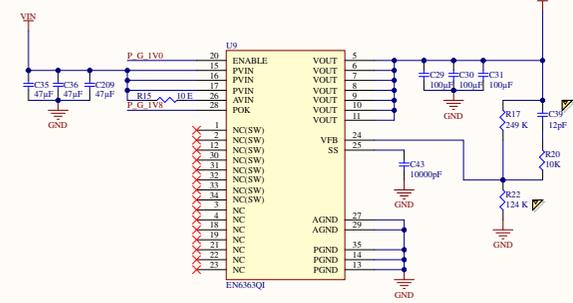
### PWR\_SELECT\_VCC0



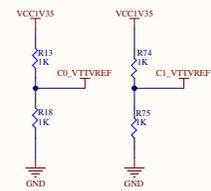
### POWER MGTAVCC



### POWER VCC1V8



### DDR VTTVREF



### VCCADC

